Programmable Logic Devices: A Test Approach for the Input/Output Blocks and Pad-to-Pin Interconnections

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Abstract

In the last few years, an increasing use of Programmable Logic Devices (PLDs) in the development of new embedded and systems-on-a-chip (SoC) solutions created the need of new test procedures for this kind of components.

Several approaches, depending on the type of PLDs used, were proposed in the literature, addressing the test of the configurable logic array, the interconnection arrays and the configuration memory. However, very little work has been done concerning the specific test of Input/Output Blocks (IOBs) and pad-to-pin bonds.

In this paper, a method aimed at covering the test of the IOBs structure in reprogrammable PLDs is proposed. The interconnections between IOBs and other components or connectors at board level are also targeted, benefiting from the availability of Boundary Scan Test (BST) cells on the IOBs of the major PLD families and from the use of "active connectors".

1. Introduction

The use of Programmable Logic Devices (PLDs), defined as an integrated circuit that can be configured by the user for a particular design implementation, endured a considerable evolution in the last few years, in terms of complexity and capacity. The first programmable logic arrays appeared in the early seventies, offering few more than a dozen of configurable logic gates. Following the famous Moore's law [1], nowadays Field Programmable Logic Array (FPGA) platforms offer gate-array-like densities of up to eight million gates and up to four embedded RISC CPUs. This huge amount of logic resources also created new challenges to the test community.

Due to the use of smaller submicron scales, which enabled a higher integration and the production of larger devices, components became more complex and, consequently, more vulnerable to manufacturing defects.

Greater miniaturization, allied to new advanced packaging and mounting technologies, enabled the assembly of components with more than a thousand pins. Lead space on new fine-pitch packages is around half a millimeter and ball space on ball grid arrays is even smaller. Because of small pin or ball space pitch, these components are more prone to assembly errors when they are mounted in printed circuit boards (PCBs).

The increasing use of this type of packages makes it difficult to employ traditional in-circuit testers, since placing a test-channel ("nail") on every electrical contact point has become impossible, accelerating the adoption of Boundary Scan Test (BST) (IEEE 1149.1 Standard [2]). More recently, the standardization of in-system programming (ISP) [3] methods contributed to intensify the interest in this test standard. ISP brings two major advantages, concerning the manipulation of components:

- on-board sockets are no longer necessary;
- the risk of damage from mechanical handling and electrostatic discharge is now much smaller.

The increasing complexity of the components, particularly of PLDs, which are the focus of this paper, and the miniaturization of their packages, originated new

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test problems. These two aspects are addressed in this paper. First, the problem of testing the IOBs of the PLDs is examined; then, in association with it, the test of the board level interconnections to and from the PLD is considered.

This paper is organized as follows: recently proposed approaches to the test of PLDs, and their suitability for the test of IOBs, are first reviewed, followed by a general description of the IOB structural implementation. The test strategy proposed for the IOBs is then presented, accompanied by a description of its implementation and limitations. The subsequent section shows how the BST infrastructure and the employ of "active connectors" may be used to test the pad-to-pin bonds and the board level interconnections.

2. Background

In recent publications, several methodologies concerning the test of PLDs, with emphasis on complex SRAM-based FPGAs, have been considered, most of them focusing on manufacturing test methodologies, and employing several Built-In Self-Test (BIST) strategies. On-line/functional test methods and structural/ application-oriented tests have also been proposed.

An FPGA approach based on BIST techniques, presented in [4, 5], proposes to set up blocks of BIST logic only during off-line test. Exploring the reprogrammability feature of FPGAs, this method presents no area overhead or performance penalty, since the BIST logic is eliminated when the circuit is reconfigured for normal operation. A slightly different BIST technique, which implies structural modifications on the original configuration memory, is proposed in [6]. When compared to similar BIST techniques, this method reduces test time and the required off-chip memory, while enabling the automation of the test process. The internal hardware level modification of the FPGA is the major disadvantage, implying the non-universality of the solution. However, in these proposals, the main focus of the test strategies presented is the logic block, and nothing is referred about the IOBs test.

An off-line non-BIST approach to test the FPGA configurable logic blocks (CLBs) is presented in [7]. After being set up with a specific test configuration, test vectors are applied to the FPGA through its IOBs, which are also used to capture the test responses. In order to achieve 100% fault coverage at CLB level, and due to the configurable characteristic of the FPGAs, different test configurations must be programmed and specific sets of test vectors applied in each case. Although IOBs are used to enable test vector application to the CLBs and response capture, nothing is mentioned concerning their own testing.

A methodology for testing the configurable logic of RAM-based FPGAs is presented in [8]. This paper shows that only eight basic test configurations are required to fully test the whole array of CLBs. In the proposed test configurations, all the CLBs have exactly the same configuration, forming a set of one-dimensional iterative arrays. The iterative arrays present a C-testability property, so the number of test configurations is fixed and independent of the size of the FPGA. The problem of testing the RAM mode of the Look-Up Tables (LUTs) using a minimum number of test configurations is addressed in [9]. In both cases, the testing of IOBs is ignored.

All these approaches require the device to be off-line, increasing fault-detection latency and the inactivity of the system where it is inserted, which may be a problem in highly fault-sensitive, mission-critical applications. To overcome these limitations, two on-line methods based on a scanning methodology are proposed in [10, 11]. The idea behind these on-line approaches is to have a relatively small portion of the chip being tested off-line (instead of the whole chip as in previous proposals), while the rest continues to carry out its normal operation. Testing is accomplished by rotating the test functions across the entire FPGA. If the functionality of a small number of FPGA elements can be replicated on another portion of the device, then those elements can be taken off-line and tested in a completely transparent way (i.e. without interrupting the device functionality). This fault scanning procedure then moves on to copy and test another set of elements, sweeping the whole FPGA, systematically testing for faults. One drawback is that in [10] a conceptual architecture, and not a commercially available FPGA, is proposed for the implementation, while in [11], in spite of the use of an available FPGA family, the system operation has to be stopped for short intervals, to allow for safe relocation of the system logic in the last tested area.

To overcome these limitations a new approach based on the active replication of the logic blocks and interconnections is presented in [12, 13]. The active resources, i.e. resources that are part of a functional block actually being used, are replicated and their functionality relocated, without stopping the operation of the system. However the testing of IOBs was also not considered. The assignment of IOBs is strictly related with the external pins, and, therefore, with the interconnections to other components or connectors at board level. The application of a rotation strategy to release IOBs for test would imply modifications on the pin assignment and the "reconfiguration" of the board level interconnections, which it is not feasible.

The use of concurrent test techniques is a possible solution, including self-checking designs, as proposed in [14], where Design-for-testability (DfT) features at design

level are considered. An algorithm that maps optimized Boolean expressions into LUTs may be used to automatically incorporate testability features into the implemented design, allowing on-line detection of faults within an FPGA. This is accomplished by using a unique set of cells, which operate on the premise of a two-rail checker, producing both the normal and complemented output, when a cell is operating correctly, and two outputs of the same value in the presence of a fault. A fault generated in an intermediate cell is propagated to the primary outputs, allowing on-line test of an FPGA-based system, including the FPGA IOBs. This method could be regarded as an error detection technique, rather than a structural or functional test approach, since it does not test the resources of the FPGA, neither considers its logic structure (instead it tries to detect the presence of faults in the current application). In a new configured application, the same defect may or may not be detected, because the new application may not use the faulty resource. Even if a faulty IOB is reused, since it could be configured as an input, an output, with or without tristate, or a bidirectional pin, a change in its functionality may prevent fault activation. If the system is always under reconfiguration, this method may lead to an intermittent fault, depending on whether or not a logic function is placed into a faulty resource and actually activates the fault.

A new application-oriented method that generates a functional test for the configured circuit, while considering the logic structure of the FPGA where it is implemented, is proposed in [15]. This method is an off--line field-oriented test to be used in a given application. Therefore, it presents the same drawbacks of the previously referred method.

The preceding analysis leads us to the conclusion that a feasible and reliable on-line test of the IOBs is not possible. Our proposal presents an off-line test method for the IOB structure and its interconnections at board level. There is no area overhead or performance penalty associated with the proposed test method, since the logic rearrangements required to implement it are eliminated when the circuit is reconfigured for its normal operation.

3. Structural testing of the IOBs

As a configurable component, any PLD pin could be used as an input, an output, a tristate output or a bidirectional pin. The output and tristate signals may be registered or not. The IOB provides a flip-flop for each of these signals and two multiplexers, whose selection line is controlled through the configuration memory, to bypass them. The input is available to the internal logic simultaneously as a registered and as a no registered input. A generic implementation of an IOB is illustrated in figure 1.

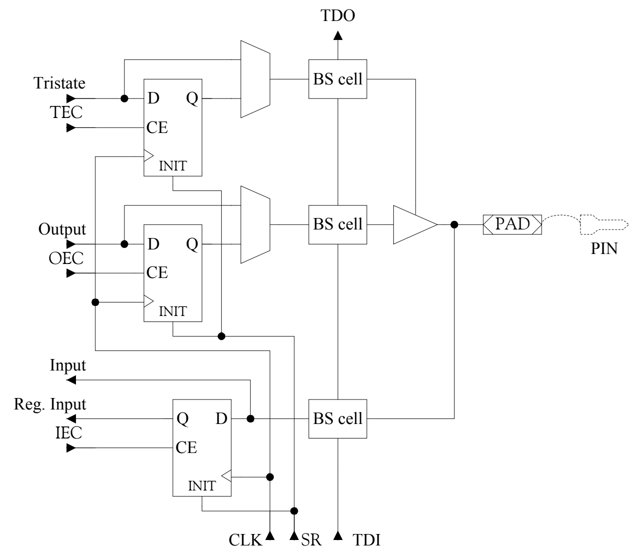

Figure 1. Internal architecture of an IOB and of its associated BS cells

In spite of the configuration of each IOB or its use (or not) to implement a system function, the number of BS cells of the BS register remains constant. All IOBs are considered independent tristate bidirectional pins, placed in a single BS scan chain. For that reason, BS cells are provided on the input, output and tristate signal paths, as required by the IEEE 1149.1 standard. Notice that, even when a bidirectional pin is only used as an input, its tristate and output BS cells stay on as part of the BS register, as well as the three BS cells of an unused bidirectional pins.

While all IOBs have a pad, as seen in figure 1, not all of them have an associated output pin. IOBs without a bond wire connecting the pad on the chip to a lead pin on the package are called unbonded IOBs. Unbonded IOBs may be used either on register intensive applications or as tristate buffers in internal bus implementations, with the bus signals being returned to the internal logic through the input path. Usually, design tools offer an option on the mapping step that enables the user to pack registers into IOBs. Despite not being true input/outputs, these IOBs have BS cells and, therefore, are part of the BS register.

Test vector application to the IOBs and response capturing should take into account the following factors:

- the BS register enables controllability of the input signal path and observability of the output and tristate signal paths;
- observability of the input signal paths and controllability of the output and tristate signal paths, and of the control and clock signals, are not possible through the BS register;
- not all IOBs have an attached pin; therefore, the external access to improve the controllability/ observability of the IOB can not be considered;

however, since they all have BS cells, this limitation is not problematic;

- PLDs compliant with the IEEE 1149.1 standard also enable the implementation of user defined registers, controlled through the BS infrastructure.

Exploring the reprogrammability feature of the FPGAs, a second BS-like register can be set up during the test phase, virtually wrapping the IOBs, and enabling total controllability/observability of their input/outputs. Implemented as a user register, it can be controlled through the BS infrastructure. No area overhead or performance penalty is implicated by this approach, since the extra register is eliminated when the circuit is reconfigured for normal operation, and no extra connections are needed to access and control it. Figure 2 illustrates the implementation of the proposed solution.

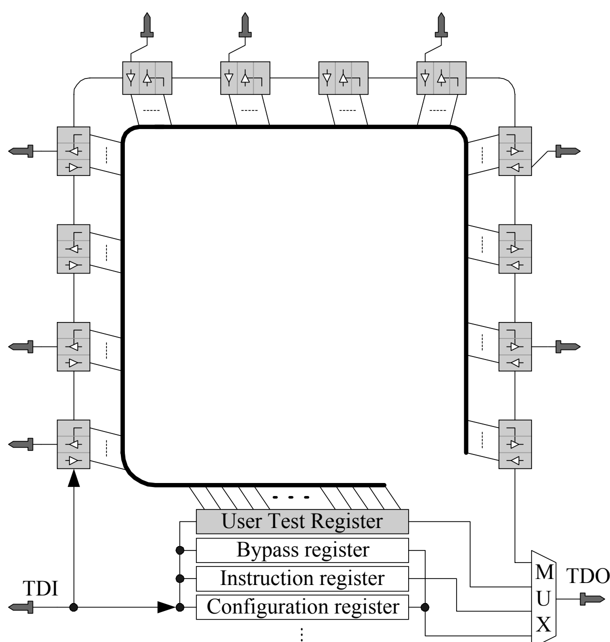

Figure 2. Infrastructure for the test of the IOBs

Each IOB, when observed from the internal side, has seven inputs and two outputs, as may be seen on figure 1. To guarantee output observability and fault diagnostic resolution, a BS-like cell must be assigned to each IOB internal output (Input and Reg. Input signals) to capture the responses to each test vector. However, test vector application (through the internal inputs) does not need to be independent for each IOB. Due to their regular structure, all internal inputs may receive the same stimulus at the same time, and thus, only seven BS-like cells are needed for the whole IOBs. The length of the BS-like register depends on the number of IOBs, which is given by

$$\#\text{"BS-like" cells} = \#\text{IOB} \times 2 + 7$$

If the number of IOBs is higher than seven, then the length of the BS-like register is lower than the length of the real BS register. As a result, the time needed to shift new values two both registers is smaller than twice the interval needed to shift the entire BS register, which is a good measure of the shorter time required to test the IOBs using this method.

The two 2-to-1 multiplexers present in each IOB are controlled through the configuration memory. For that reason, the multiplexer test requires the use of two test configurations. Additionally, the flip-flop can have is value initialized at ‘0’ or ‘1’, depending on the initialization bit programmed in the configuration memory. Notice that only one initialization line (SR in figure 1) is available to set or reset the flip-flop. Therefore, the complete test of the IOBs’ structure implies the use of a minimum of three test configurations, independently of the PLD size. The reconfiguration of the IOBs can also be achieved through the BS interface, exploiting the ISP features available in the PLDs.

Because the internal structure implementation of the multiplexers and flip-flops is not known, a hybrid (functional/stuck-at) single fault model is used for the generation of the test vectors, based on the conclusions presented in [8]. Table 1 shows the 13 test vectors to be shifted through the User Test Register, generated to test each flip-flop+multiplexer set, and the expected result. They are divided in three groups, depending on the value assigned in the configuration memory to the multiplexer selection input, and to the flip-flop initialization value. These elements are part of the output and tristate paths, while the input path has no multiplexer, thus the first two vectors do not need to be shifted through the BS register. The test vectors are subsequently shifted to both registers, BS and User Test.

CLK	SR	CE	D	Output
Mux select=0 INIT=0				
0	0	0	0	0
0	0	0	1	1
Mux select=1 INIT=0				
0	1	0	1	1
1	1	0	1	0
1	0	0	1	0
0	0	0	1	0
1	0	0	1	0
1	0	1	0	0
0	0	1	0	0
1	0	1	0	0
Mux select=1 INIT=1				
1	1	1	0	0
0	1	1	0	0
1	1	1	0	1

Table 1. Test vectors

For the implementation of this method, a simple BS controller is needed for test vector application and response capturing, and to perform the configuration of the test configurations. An expensive Automatic Testing Equipment (ATE) will not be necessary.

4. Testing the PLD interconnections at board level

One of the limitations of the proposed method is its inability to assure that the bond wire is not broken or incorrectly positioned, leading to a defective connection. As chip and packages shrink, the possibility of bonding defects increases. Even after assembly, mechanical stress due to component manipulation may lead to bond or solder breaking.

The test of the bond wires requires the use of some kind of external tester, since it is essential to access the external pin, in order to assure its continuity.

Current integration levels vastly increased the availability and versatility of resources in the newest PLDs, enabling the implementation of the concept of systems-on-a-chip (SoC). Generic PLD boards do not have more than a few components to manage power supply, implement the communications interface, and – sometimes – a memory to store the PLD configuration. These components do not have any associated test infrastructure, which makes it difficult to test the bond wires. Finally, all boards have connectors with hundreds of pins. One of the possibilities to access the component is through these connectors. However, this solution implies the availability of hundreds of test channels synchronized with the on-board BS infrastructure, which is hardly feasible.

One solution to this problem is the use of "active connectors", as presented in [16, 17]. An "active connector" is a transparent connector made up of a set of BS cells, as represented in figure 3.

Instead of interconnecting each input or output to a tester channel, an "active connector" is placed after the normal connector, establishing a BS chain around the board. From the tester's viewpoint the board behaves as another component interconnected with the PLD.

In generic PLD boards, with almost all PLD pins directly connected to the edge connectors, this approach presents the advantage of integrating the test of primary Input/Output pins through the BS infrastructure. Apart from covering the test of bond wires, it also enables the test of the board interconnections, which are often distributed by several inaccessible layers. The implementation of the whole solution is represented in figure 4. No extra hardware or modifications are required at board level.

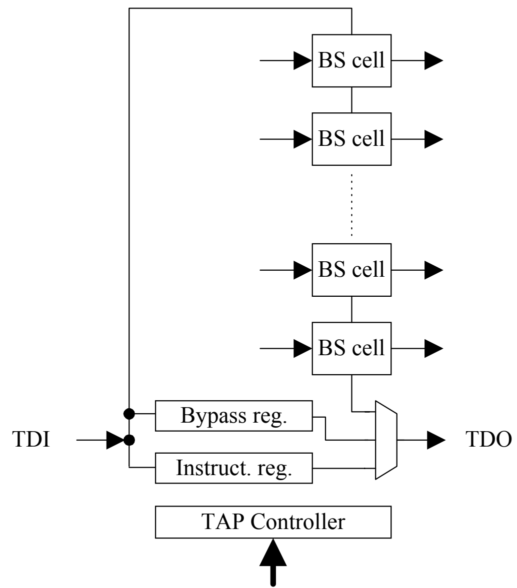

Figure 3. An active connector

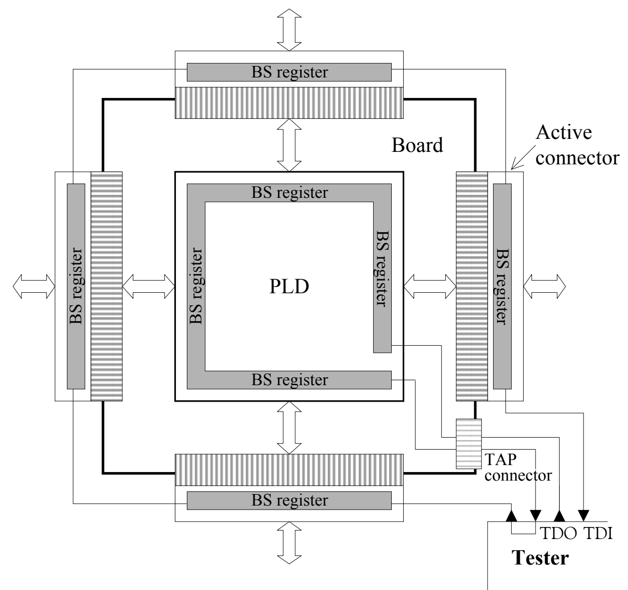

Figure 4. Implementation of the proposed solution

The length of the BS chain implemented through the active connectors is much smaller than the length of the PLD BS chain. Each PLD IOB has three BS cells, but each bonded pin connects to only one edge connector pin. If all of the PLD IOBs were bonded IOBs, the length of the BS chain of the active connectors would be a third of the length of the PLD BS chain. By example, a XCV200 FPGA from Xilinx in a BG352 package has 336 IOBs, and a total of 1022 BS cells, but only 260 I/O pins are available externally and can be routed to an edge connector. Assuming one BS cell assigned to each pin

connector, we may conclude that the length of the active connector BS chain is around 25% the length of the PLD BS chain, which generates a small test time overhead.

5. Conclusion

This paper presented a solution to the problem of testing the IOBs of reprogrammable or reconfigurable devices comprising a BS infrastructure. The test of the internal structure of the IOBs is accomplished by configuring a User Test Register that exists only while the test takes place. There is no area overhead implied by the application of the method, since the extra register is eliminated when the circuit is reconfigured for normal operation. The reduced number of test configurations is also a good indication of the short time required to test the IOBs.

Due to the regular structure of IOBs, test pattern generation has a very low complexity and is performed for a single flip-flop+multiplexer set. Fault location is resolved to a single set of these elements.

The use of "active connectors" enables the test of pad--to-pin bonds and, additionally, of the PCB lines interconnecting the PLD to the edge connectors, without requiring expensive testers.

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