A Novel Methodology for the Concurrent Test of Partial and Dynamically Reconfigurable SRAM-based FPGAs

Manuel G. Gericota, Gustavo R. Alves
Department of Electrical Engineering - ISEP
Rua Dr. António Bernardino de Almeida - 4200-072 Porto - PORTUGAL

Miguel L. Silva, José M. Ferreira
Department of Computers and Electrical Engineering - FEUP
Rua Dr. Roberto Frias - 4200-465 Porto – PORTUGAL

Abstract

This poster presents the first truly non-intrusive structural concurrent test approach, aimed to test partial and dynamically reconfigurable SRAM-based FPGAs without disturbing its operation. This is accomplished by using a new methodology to carry out the replication of active Configurable Logic Blocks (CLBs), i.e. CLBs that are part of an implemented function that is actually being used by the system, releasing it to be tested in a way that is completely transparent to the system.

1: Introduction

Many of the trends that make newer FPGAs more appealing and affordable also make them less reliable. Larger dies and the use of smaller sub-micron scales in its manufacturing increase the probability of lifetime operation failures, claiming for new test / fault tolerance methods, capable of assuring the reliability of the system.

A higher reliability level can therefore only be achieved via the continuous test of all FPGA blocks throughout the system lifetime, and by the introduction of fault tolerance features. The same run-time partial reconfiguration features that originated this test challenge enable the development of a novel structural test method with the following main characteristics: i) it is the first truly non--intrusive test method proposed in the literature; ii) it is able to detect any permanent failures emerging during system lifetime; iii) no FPGA I/O pins are occupied with test functions, since its complete implementation is based on the Boundary Scan (BS) infrastructure (IEEE 1149.1). While testing the CLBs, our procedure also enables a significant fraction of all available routing resources to be tested as well.

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2: The DRAFT method

In the vast majority of reconfigurable hardware systems, multiple independent hardware blocks share the same FPGA device dynamically, at the same time. Nevertheless, 100% usage of the FPGA resources is hardly ever achieved, so a few blocks will always be free.

The DRAFT (Dynamically Rotate And Free for Test) method, presented in [1], is based in a scanning technique where temporarily unused FPGA CLBs are structurally tested without disturbing system operation, taking advantage of new FPGA partial and dynamic reconfigurable features. Using a two-step dynamic replication method, CLBs currently being used by a given application can have their functionality dynamically replicated in one of the CLBs already tested. This process eliminates any fault affecting the value presented in the flip-flops since the state values for the CLB replica are acquired directly from its inputs. After transferring its functionality, the replicated CLB is free to be tested. Carrying out a rotation scheme that covers the whole FPGA, this solution guarantees its complete test. Run-time partial reconfiguration, test application and response capturing is accomplished through the BS infrastructure without ever stopping the system clock. This method also enables the implementation of fault tolerance features, with the CLBs eventually found defective being replaced by successfully tested spare ones. Since our solution is able to dynamically tolerate faults in the field, the system can still operate in the presence of faulty CLBs, and reliability is improved with reasonably low hardware redundancy.

References

[1] M. G. Gericota, G. R. Alves, M. L. Silva, J. M. Ferreira, "DRAFT: An On-Line Fault Detection Method for Dynamic and Partially Reconfigurable FPGAs", *Proc. of the 7th IEEE On-Line Testing Workshop*, July 2001, pp. 34-36.