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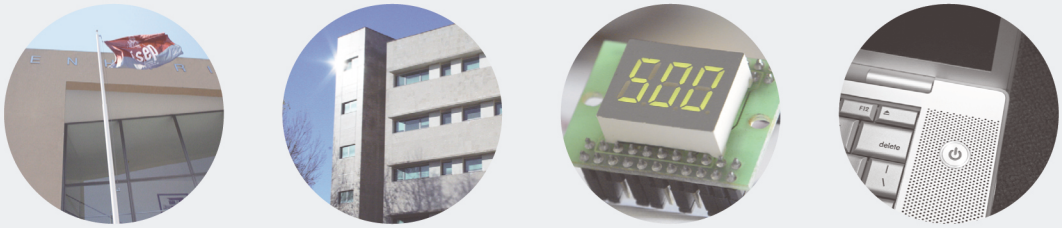

Controller Implementation Using Analog Reconfigurable Hardware (FPAA)

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DO PORTO

CONTROLLER IMPLEMENTATION USING ANALOG RECONFIGURABLE HARDWARE (FPAA)

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This report fulfil, partially, the needs that are in the Unit Course of Thesis, of the 2º year, of Master in Computer and Electrical Engineering

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To my Parents

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I would also like to give my kindly regards to my parents for the support provided during the period of this work.

I am thankful to Mr. Antonio for mechanical support to build the temperature chamber.

Abstract

This Thesis has the main target to make a research about FPAA/dpASPs devices and technologies applied to control systems. These devices provide easy way to emulate analog circuits that can be reconfigurable by programming tools from manufactures and in case of dpASPs are able to be dynamically reconfigurable on the fly. It is described different kinds of technologies commercially available and also academic projects from researcher groups.

These technologies are very recent and are in ramp up development to achieve a level of flexibility and integration to penetrate more easily the market.

As occurs with CPLD/FPGAs, the FPAA/dpASPs technologies have the target to increase the productivity, reducing the development time and make easier future hardware reconfigurations reducing the costs.

FPAA/dpAsps still have some limitations comparing with the classic analog circuits due to lower working frequencies and emulation of complex circuits that require more components inside the integrated circuit. However, they have great advantages in sensor signal condition, filter circuits and control systems.

This thesis focuses practical implementations of these technologies to control system PID controllers. The result of the experiments confirms the efficacy of FPAA/dpASPs on signal condition and control systems.

Keywords

FPAA, dpASP, CAB, CAM, AMPOP, VLSI, OTA, CPLD, FPGA, PID, OTA, SC.

Resumo

Esta tese tem como principal objectivo fazer uma pesquisa sobre circuitos integrados e tecnologias das FPAA/dpASPs aplicadas a sistemas de controlo. Estes dispositivos possibilitam a emulação de circuitos analógicos que podem ser reconfiguráveis por ferramentas de programação dos próprios fabricantes e no caso dos dpASPs são capazes de ser dinamicamente reconfiguráveis em tempo real. São descritas diferentes tecnologias disponíveis no mercado e também projectos académicos de grupos de investigação.

Estas tecnologias são muito recentes e estão em pleno desenvolvimento para alcançar um nível de flexibilidade e integração para penetrar mais facilmente no mercado.

Como já ocorre com as CPLD/FPGAs, os FPAA/dpASPs tem o objectivo de aumentar a produtividade, reduzindo o tempo de desenvolvimento e facilitar reconfigurações futuras de hardware, reduzindo os custos.

As FPAA/dpASPs ainda tem algumas limitações comparando com os circuitos analógicos clássicos devido a uma menor largura de banda de frequências de trabalho e à dificuldade de emulação de circuitos complexos que requerem mais componentes dentro do circuito integrado e portanto uma maior escala de integração. No entanto, estes circuitos integrados têm grandes vantagens e podem ser utilizados para aplicações de condicionamento do sinal de sensores, circuitos de filtros e sistemas de controlo.

Esta tese concentra-se nas implementações práticas destas tecnologias aos sistemas de controlo usando controladores PID. Os resultados das experiências confirmam a eficácia das FPAA/dpASPs no condicionamento de sinal e sistemas de controlo.

Palavras-Chave

FPAA, dpASP, CAB, CAM, AMPOP, VLSI, OTA, CPLD, FPGA, PID, OTA, SC.

Contents

List of Figures

Index of Tables

Acronyms

ADC – Analogic Digital Converter

AFGA – Auto Zeroing Floating Gate Amplifier

ARM – Acorn RISC Machine architecture

ASCII – American Standard Code for Information Interchange

ASIC – Application Specific Integrated Circuit

BiCMOS – Bipolar Complementary Metal Oxide Semiconductor

CAB – Configurable Analogue Block

CAM – Configurable Analog Modules

CC – Current Conveyor

CPU – Communication Processor Unit

CRC – Cyclic Redundancy Check

CADSP – Cooperative Analog Digital Signal Processing from Giorgia Tech

COP – Coefficient of Performance

CPLD – Complex Programmable Logic Devices

CT – Continuous Time

CTBm – Continuous Time Block mini

DAC – Digital Analog Converter

dpASP – Dynamic Programmable Analog Signal Processor

ELIN – Externally Linear Internally Non Linear

EEPROM – Electrically Erasable Programmable Read Only Memory

E2CMOS – Electrically Erasable Complementary Metal Oxide Semiconductor

FET – Field Effect Transistor

FB – Function Block

FPAA – Field Programmable Analog Array

FPGA – Field Programmable Gate Array

GaAs – Gallium Arsenide

GPIO – General Propose Input Output

IC – Integrated Circuit

IEEE – Institute of Electrical and Electronics Engineers

IMTEK – Department of Microsystems Engineering frome University of Freiburg

I/O – Input Output

ISP – In System Programmable

JTAG – Joint Test Action Group

LUT – Look Up Table

LVDT – Linear Voltage Differential Transformer

MOS – Metal Oxide Semiconductor

MITE – Multiple Input Trans-linear Element

nFET – Negative Field Effect Transistor

NTC – Negative Temperature Coefficient

OPAMP – Operational Amplifier

OTA – Operational Transcondutance Amplifier

OTA-C – Operational Trancondutance Amplifier - Capacitor

PC – Personal Computer

PCB – Printed Circuit Board

PIC – Programmable Intelligent Computer

PID – Proportional Integral Differential

PGA – Programmable Gain Amplifier

pFET – positive Field effect transistor

PROM – Programmable read-only memory

PSIM – Power Simulator software

PSoc – Programmable System on chip

RASP – Reconfigurable Analog Signal Processor

RC – Resistor Capacitor

R&D – Research and Development

RF – Radio Frequency

RFID – Radio Frequency IDentification

SAR – Successive Approximation Register

SC – Switch Capacitor

SC/CT – Switched Capacitor / Continuous Time

SPDT – Single-Pole, Double-Throw

SPI – Serial Peripheral Interface

SPST – Single-Pole, Single-Throw

SI – Switch Current

SOC – System On Chip

SOS – Second Order Section

SRAM – Static random-access memory

TEA – Thermoelectric Assembly

TEC – Thermoelectric Cooler

TSMC – Taiwan Semiconductor Manufacturing Corporation

UART – Universal Asynchronous Receiver/Transmitter

USB – Universal Serial Bus

VLSI – Very Large Scale Integration

VMR – Voltage Main Reference

ZIF – Zero Insertion Force

1. INTRODUCTION

This chapter presents the project motivation, its main objectives and the schedule followed by the report structure.

1.1. CONTEXTUALIZATION

Reconfigurable hardware devices in the field of analog signals have been of great interest to designers and hardware manufacturers. The creation of analog systems is still complex, combined with long periods of tests and evaluations.

The appearance of the CPLD/FPGAs have revolutionized the development of digital circuits and similarly situation is occurring with FPAA/dpADP technologies, which provides interfaces and resources for development of analog systems (signal conditioning, filters, PID controllers, adders, multipliers, sample-and-hold, etc.) based on operational amplifiers and other analog circuits which can easily be changed without reconstructing the circuit or replacement of electronic components.

These technologies are in development process and are focused on the following areas: signal conditioning and sensor interface; filtering conditioning designs, automation and industrial control, monitoring and medical diagnostics, control accuracy, conditioning ultra-low frequency signals, RFID systems, etc.

1.2. SCOPE AND PURPOSES

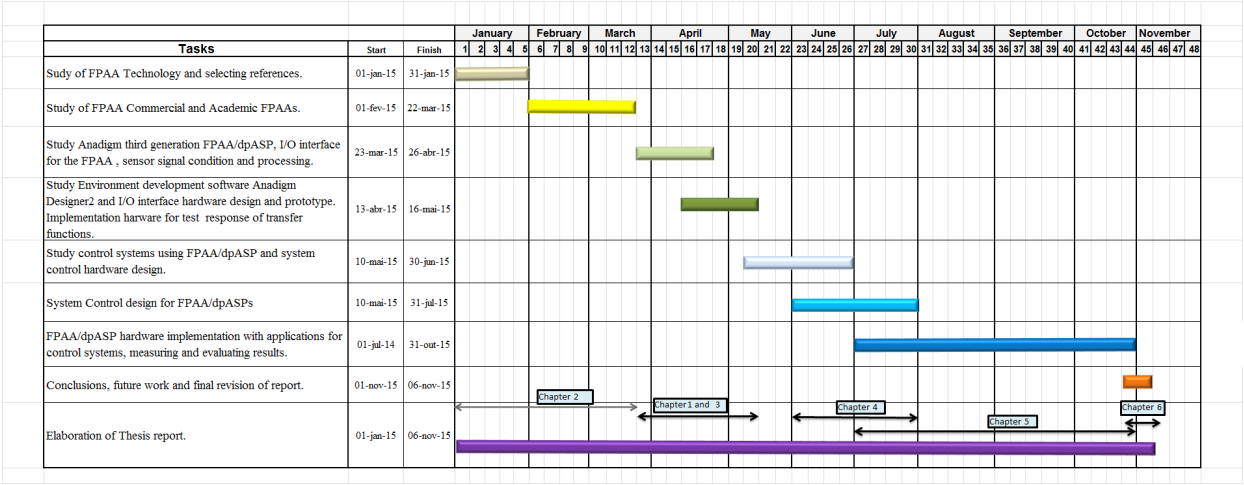
The real propose of this work is to explore the potentialities of reconfigurable analog hardware using FPAA/dpASPs applied to control systems. The main objective is to describe the technologies from these IC devices and study their performance in the signal conditioning and system control. The main activities to accomplish this task are the following:

- Study of discrete time and continuous time base technologies used in FPAA design and their main characteristics and comparison between them.
- Study the development of FPAA /dpASPs and technology comparison between the IC devices from manufacturers.
- Describe two academic FPAA development projects from researcher groups.
- Describe the operation of an FPAA/dpASP from a main manufacturer, Anadigm.
- Study of the applicability of FPPA/dpASPs in sensor signal conditioning and processing and control systems.
- Realize its advantages and disadvantages compared to classical techniques of realization of analog circuits.
- Implementation of practical circuits with FPAA/dpASPs, focus on applications in sensor signal conditioning, transfer function simulation and control systems.
- Practical application of PID controller using FPAA/dpASPs to control temperature inside chamber in terms of cooling and heating.

1.3. SCHEDULE

In Table 1.1, it is possible to observe the scheduling concerning the tasks performed during the development of this Thesis.

Table 1.1 Work Thesis Schedule.



1.4. OUTLINE OF THESIS

This thesis is organized as follows.

Chapter 2, introduces the technologies to implement the FPAAs. It was consulted extensive bibliography regarding various types of FPAAs produced by different manufacturers and as well two examples from academic researcher groups based on two different technologies, continuous-time and discrete-time. Their advantages and disadvantages were studied compared to traditional mounting analog circuitry using passive components. Finally, it was focus on internal block description of third generation FPAA/dpASPs from Anadigm that is used on the Thesis for control applications.

Chapter 3, describes the development board used on this Thesis from Anadigm. It is mentioned several methods for the I/O board interface and applications in the domain of signal conditioning and transfer function response. Also, it is explained the main functions of development programming software and operation of the FPAA/dpASPs Anadigm devices. Finally, it is shown some examples of hardware implementations of transfer functions, comparing results from simulator with practical results obtained by measurement instrumentation.

Chapter 4, presents tuning rules for PID controller parameters putting focus on Ziegler-Nichols first and second methods. It is described the PID design implementation on dpASP/FPAA hardware technology. Finally it is simulated a second order plant process on a FPAA and implemented in a PID design on two FPAA in closed-loop with the transfer function implemented on third FPAA. Then is obtained the step response for diverse PID parameters on simulator and compared with result on MATLAB.

Chapter 5, describes the project application of PI controller design implemented on dpASP/FPAA to control temperature inside chamber for cooling process using Peltier thermoelectric assembly and heating process using flexible silicone heaters.

Chapter 6, presents the conclusion with positive aspects of using this technology on PID control systems and future work development.

2. FPAA–ARCHITECTURES AND TECHNOLOGIES

The trend in modern Very Large Scale Integration (VLSI) circuit design is to increase the level of integration, decrease the time of design and development and reduce the cost of products. The key concept is to use a single hardware implementation for more than one type of system by reprogramming it for different systems in the field; this type of re-configurability can be achieved by programmability. The need of programmability and re-configurability has led to the use of field programmable arrays.

The field programmable arrays on digital domain are implemented by using de Complex Programmable Logic Devices (CPLDs) and Field Programmable Gate Arrays (FPGAs). These devices allow digital hardware prototypes very quickly and reduce costs of the final products as the development time is reduced. They have advantage of increasing the flexibility to perform updates after release the products to the market.

In case of high volume production, the cost from the conception until the production is lower using Application Specific Integrated Circuits (ASICS). However, these devices do not have the flexibility of re-configurability and hardware configuration updates are not

possible after release them to the market in counterpart with FPGAs that allow the re-configurability of the hardware.

The programmable and reconfigurable devices able to perform signal processing in the analog domain had a slower evolution comparing with the digital domain devices. Only in the decade of 1980's, occurred some growth in the development of these devices. The Field Programmable Analog Arrays (FPAAs) appeared for the first time commercially in the decade of 1990's.

Analogue signal processing is normally preferred in high-speed and low-power applications. For many signal processing applications, analogue Integrated Circuits (ICs) require a smaller chip area and lower power consumption than their digital counterparts, mainly due to the lack of requirements for anti-aliasing and post-smoothing filters and analogic to digital (A/D) and digital to analog (D/A) signal converters.

There are fundamental difficulties in realizing universal FPAAs over FPGAs. Apart from those well-known challenges such as linearity, noise and bandwidth subjects and environmental variations, the configurable analogue blocks in the FPAA must provide a number of programmable functions and the configurable routing should not decrease the accuracy of the implemented circuit. Research in FPAAs and their applications has attracted substantial interest across the whole IC sector including both academic research and industry.

2.1 GENERAL ARCHITECTURE

FPAAs contain an array of programmable function blocks (FB) or configurable analogue blocks (CAB), which can be reconfigured or reprogrammed for different analogue signal processing functions with aid of the programmable interconnection network. Both FB/CAB and interconnection network can be programmed by on-chip memory.

The software for particular FPAA chip enables the user to design and simulate analogue applications and then send and write the data to the FPAA hardware to program the device. The generic block diagram of an FPAA is shown in Figure 2.1.

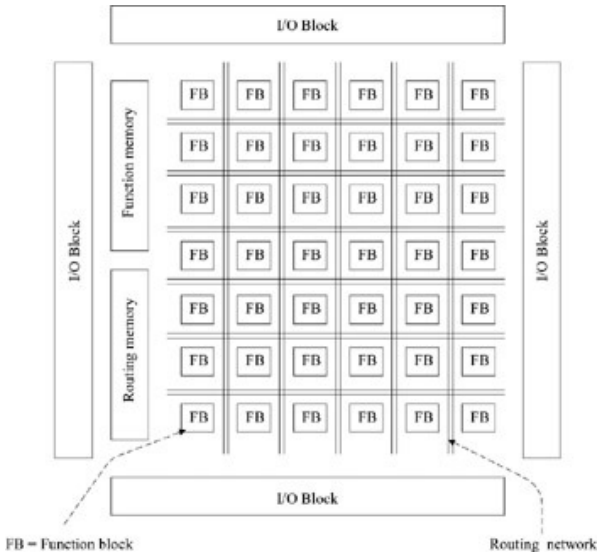


Figure 2.1Generic FPAA architecture [3].

The routing memory stores a bit string which is used for the connectivity of the interconnection network, and the function memory stores a bit string which is used for function generation of the FB/CABs and fine tuning of function parameters.

Interconnection networks can take the form of a tree, crossbar or data path, which connect the FB/CABs and input/output signals for different given system requirements. Each FB/CAB can be programmed to implement some basic analogue functions such as adders, multipliers, amplifiers, integrators, etc. FB/CABs can be designed for both specialized and general purpose FPAAs.

The I/O blocks are arranged surrounding all the four sides of the array to provide the input and output interface for the chip.

2.2 TECHNOLOGICAL CLASSIFICATION

In the time domain, analog signals can be divided into two classes: continuous-time signals and discrete-time signals. The division of analog signals into discrete-time and continuous-time signals is important because it determines the main classification of reconfigurable circuits.

Analog reconfigurable devices are classified in two types according the working methodology:

- The discrete time class of reconfigurable circuits is mainly based on the Switched Capacitors (SC) or Switched Current (SI) principle.

- The continuous time class of reconfigurable circuits contains devices based on Operational Transconductance Amplifiers (OTA), current conveyors (CC), Active resistor-capacitor (RC) circuits and a class of Externally Linear Internally Non Linear circuits (ELIN), as example the log domain circuits, square root domain circuits and others.

The mixed mode of reconfigurable circuits uses the two technologies and usually contains a continuous time tunable anti-aliasing filter at the input, a fully reconfigurable SC network as a processing unit and a continuous time smoothing filter at the output. However, sometimes they contain also both – continuous time and discrete time processing blocks.

The continuous time design techniques provide higher bandwidth, lower power consumption and smaller area of the integrated circuit IC die chip. On the other hand, the discrete time switched circuit techniques provide easier programming and less sensitivity to variances in the manufacturing process but consume more power and is limited to a lower bandwidth of operation, occupying higher area of the IC die chip due to include anti-aliasing and sample-and-hold circuits [4,5].

2.2.1 DISCRETE TIME TECHNOLOGY

Discrete time FPAAs use frequently SC techniques. This type of circuits is based on MOS switches, capacitors and Operational Amplifiers (OPAMPs).

The active devices using MOS technology are able to implement switches, OPAMPS, capacitors with low level of capacity and small level resistors. However, this technology does not implement resistors with values of 1 KΩ or higher and capacitors with values higher than 1 nF with accuracies less than 1%.

To overcome this technological difficulty, it is explored the development of SC circuits to emulate devices as the resistors, simulated by using periodically operated MOS switches and capacitors. Such circuits are especially attractive for realization using VLSI

technologies which the basic elements are MOS transistors and capacitors in the pico Farad range.

An advantage of SC technology is that resistors are eliminated. However SC requires large amount of die area and power consumption and they have high tolerances which is not acceptable for chip design.

A disadvantage of SC circuits is the noise included by spurious high-frequency responses due to the nature of the sampling processes. This disadvantage is reduced by using a clock frequency that is much higher than the highest signal frequency component.

A SC circuit realization of a resistor could be modeled with single-pole, double-throw (SPDT) switch, shown in Figure 2a) and the correspondent equivalent resistor in Figure 2b).

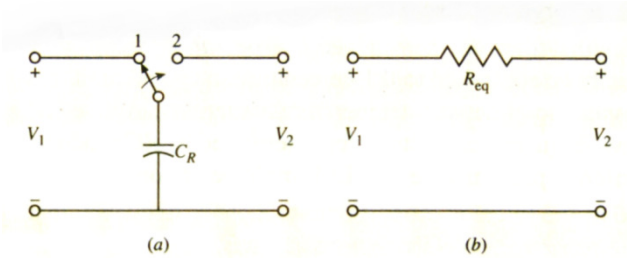


Figure 2.2a) SC circuit to simulate a resistor; b) Equivalent resistor [2].

With the switch at the left position (position 1), the capacitor C_R charges to the voltage V_1.The charge on C_R has the value Q_1:

$$Q_1 = C_R \times V_1 \tag{2.1}$$

When the switch is moved to the right (position 2), C_R discharges until the voltage value reaches V_2. Now, the charge on C_R has the value Q_2:

$$Q_2 = C_R \times V_2 \tag{2.2}$$

The net charge transfer per cycle of the switch is:

$$\Delta Q = Q_1 - Q_2 = C_R \times (V_1 - V_2) \tag{2.3}$$

Considering the switch cycles back and forth at frequency f_C, the correspondent period T_c is the following:

$$T_C = \frac{1}{f_C} \tag{2.4}$$

The average current assuming constant values of V_1 and V_2 is the following:

$$Iavg = \frac{\Delta Q}{\Delta T} = \frac{\Delta Q}{\Delta T_C} = C_R \times f_C \times (V_1 - V_2) \tag{2.5}$$

If f_C is much higher than the highest frequency component in V_1 and V_2, then the transfer process may be treated as a continuous and the switched capacitor circuit shown in Figure 2.2a) may be modeled as an equivalent resistor as shown in Figure 2.2b), where:

$$R_{eq} = \frac{V_1 - V_2}{Iavg} = \frac{1}{C_R \times f_C} \tag{2.6}$$

The circuit shown in Figure 2.2a) could be modified replacing the SPDT switch with two single-pole, single-throw (SPST) switches as shown in Figure 2.3a).

To describe the working sequence of these switches, it is used the time diagram in Figure 2.3b). It consists of two MOS switches, switch 1 and switch 2 driven by clock voltage waveforms $\emptyset_1$ and $\emptyset_2$.

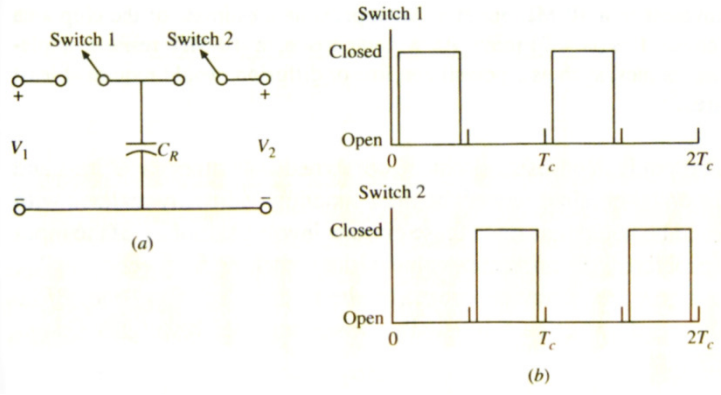


Figure 2.3a) SC circuit with two single-pole single-throw (SPST) switches; b) Clock signals [1].

Figure 2.4a) shows the equivalent circuit with two MOS transistors and capacitor C_R. The implementation of such an equivalent resistor is very attractive in VLSI technology because it provides very effective usage of silicon chip area. Figure 2.4b) shows the clock signals applied to the gates of MOS transistors, $\emptyset_1$ and $\emptyset_2$.

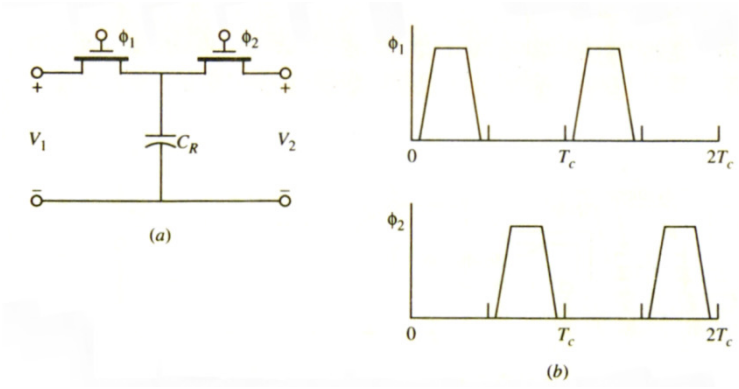


Figure 2.4a) MOS implementation of SC resistor; b) Clock signals applied to the gates [2].

To avoid the two MOS transistors to conduce at same time on the transition of the clock signals, the waveforms of $\emptyset_1$ and $\emptyset_2$ shown on Figure 5 applied to the gates are type non-over-lapping, which ensures that the first MOS transistor passes to the OFF state before the second MOS transistor passes to ON state. This technique is named break-before-make.

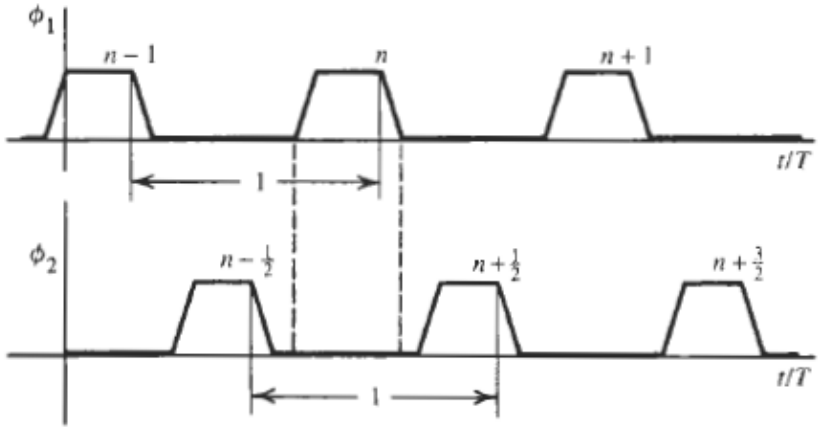


Figure 2.5 Two phase non-overlapping clocks [6].

The clock signal $\emptyset_1$ is noted with pulse positions at $n-1,\ n,\ n+1$, etc. The clock signal $\emptyset_2$ is noted with pulse positions at $n-\frac{1}{2},\ n+\frac{1}{2},\ n+\frac{3}{2}$, etc.

The SC circuit equivalent resistor can be combined in configurations together with other capacitors and OPAMPs to obtain many specialized circuits like filter functions normally realized with active RC filter circuits.

It should be considered that F_{Cmin} used for switching clock of the gate MOS transistors is according the Nyquist frequency:

$$F_{Cmin} = 2 \times f_0 \tag{2.7}$$

Where f_0 is the maximum frequency component of the signal sampled of V_1. In practice, f_0 is usually higher and it is very common use the following Fc value:

$$F_C = 100 \times f_0 \tag{2.8}$$

In order to minimize the silicon chip area required for a given switched capacitor circuit implementation, the capacitor values used in the design are usually quite small, on the order of a few pF. For such values, the effects of parasitic capacitances become very significant. The parasitic capacitance of all internal interconnections of the MOS transistors can be modeled by a single capacitor C_P as shown in Figure 2.6.

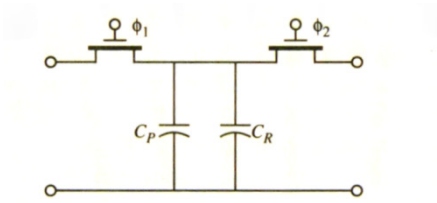


Figure 2.6 Parasitic capacitance C_P on a MOS transistor [2].

Since C_P may be as much as 20 % of the value of C_R, considerable error can be introduced into circuit realization by ignoring it. Compensate the C_P effect by simply making the sum of $C_R + C_P$ equal to the desired value is not practical due the value of C_P is not easily determined and may vary considerably due to its nonlinear behavior.

To provide a compensation for parasitic effects in the SC implementation, the SPDT switch shown on previous Figure 2.2a) is replaced by a pair of SPDT switches as shown in Figure 2.7a) and the correspondent circuit with MOS transistors in Figure 2.7b). An implementation of the dual switch circuit, the parasitic capacitor C_P is converted in two capacitors C_{P1} and C_{P2}. When the two switches are in position 1 corresponding to $\emptyset_1$ high, the charge on C_R is given by the expression:

$$Q_1 = C_R \times (V_1 - V_2) \tag{2.9}$$

When the two switches are in position 2 corresponding with $\emptyset_2$ high, C_R is discharged. In addition, the parasitic capacitors C_{P1} and C_{P2} are discharged and have no effect on the voltages V_1 and V_2. The charge transferred per cycle of the switch is:

$$\Delta Q = C_R \times (V_1 - V_2) \tag{2.10}$$

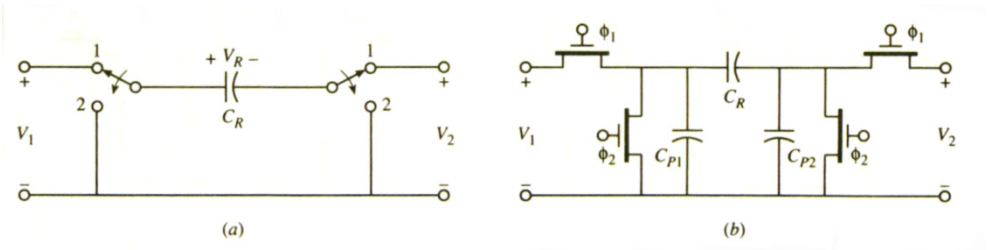


Figure 2.7 a) SC circuit of resistor with SPDT switches; b) Parasitic insensitive, MOS SC circuit [2].

A modification of the two-switch design in previous Figure 2.7a) and Figure 2.7b) is shown on Figure 2.8a) and Figure 2.8b). In the most frequently used application circuit, the right terminal V_2 is connected to the inverting input of an OPAMP, this means at zero potential. In this case V_2= 0 V and if the switching cycle is repeated at a frequency Fc, then circuit provides a parasitic insensitive implementation for a negative value resistor. The equivalent resistor value is:

$$Req = -\frac{1}{C_R \times Fc} \tag{2.11}$$

This circuit is very useful to implement a non-inverting SC integrator.

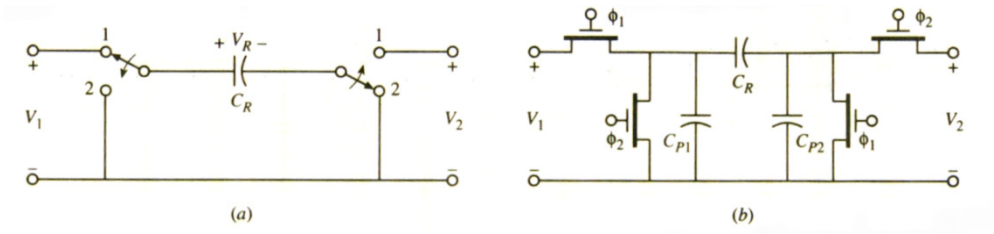


Figure 2.8a) SC circuit of negative resistor with SPDT switches; b) Parasitic insensitive SC equivalent negative resistor with MOS transistors [2].

The following basic SC circuit is the integrator configured as inverter integrator. The transfer function of the RC active circuit configuration shown on Figure 2.9a) is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-1}{s \times R_1 \times C_2} \tag{2.12}$$

For the SC inverter integrator, with correspondent MOS switch circuit representation on Figure 2.9b), the transfer function is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-C_1 \times fc}{s \times C_2} \tag{2.13}$$

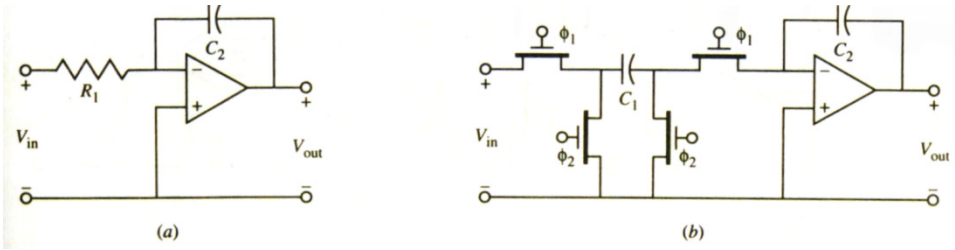


Figure 2.9a) RC inverter integrator; b) SC equivalent [2].

The non-inverting integrator in the active RC circuit shown in Figure 2.10a) is implemented by the correspondent SC MOS circuit on Figure 2.10b).

The voltage transfer function of RC circuit is the following:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{s \times R_1 \times C_2} \tag{2.14}$$

For the SC non inverter integrator, the correspondent MOS switch circuit representation has the following transfer function:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{C_1 \times fc}{s \times C_2} \tag{2.15}$$

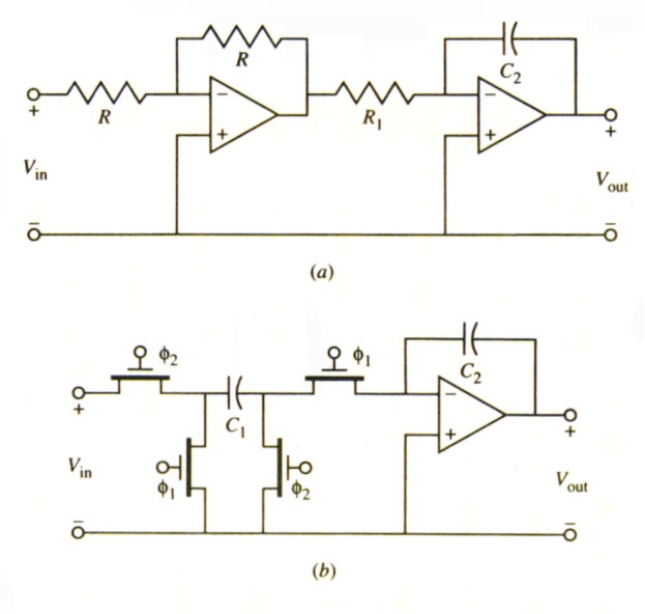


Figure 2.10 a) RC non-inverting integrator; b) SC equivalent circuit [2].

A first order SC circuit is shown in Figure 2.11. The equivalent resistances R_2 and R_3 are simulated by the SC circuits with C_2 and C_3. The voltage transfer function is the following:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{s \times C_1 + fc \times C_2}{s \times C_F \times f_{C\times} C_3} \tag{2.16}$$

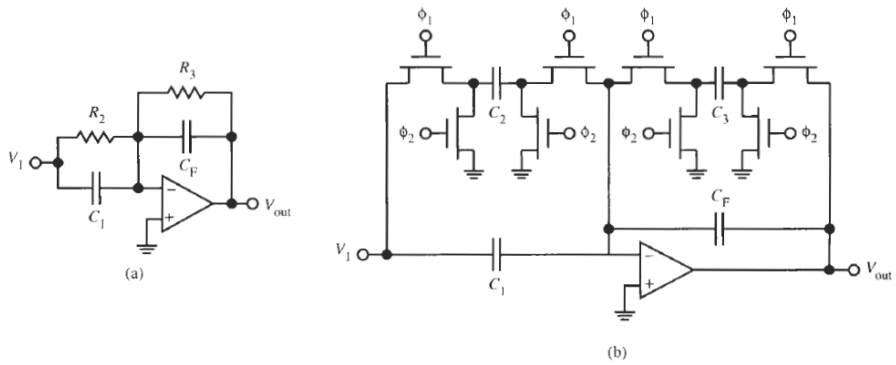


Figure 2.11 a) RC first order circuit; b) SC equivalent circuit [6].

A second-order SC filter can be synthesized using a two-integrator loop, such as the biquadratic configuration of RC prototype shown on Figure 2.12. It is a biquadratic filter that consists of a loss inverting integrator followed by a lossless inverting integrator and a unity-gain inverting amplifier whose main propose is to provide a polarity inverting.

The combined function of the last two blocks is loss less no inverting integration, which can be synthesized in SC form using only one OPAMP. Therefore, the SC version of the biquadratic requires only two OPAMPs, one to provide differencing, loss inverting integration, and the other to provide lossless non-inverting integration as shows Figure 2.13. This circuit represents a SC Tow-Thomas filter. For stray-insensitive performance, C_3 can be operated with a dual switch.

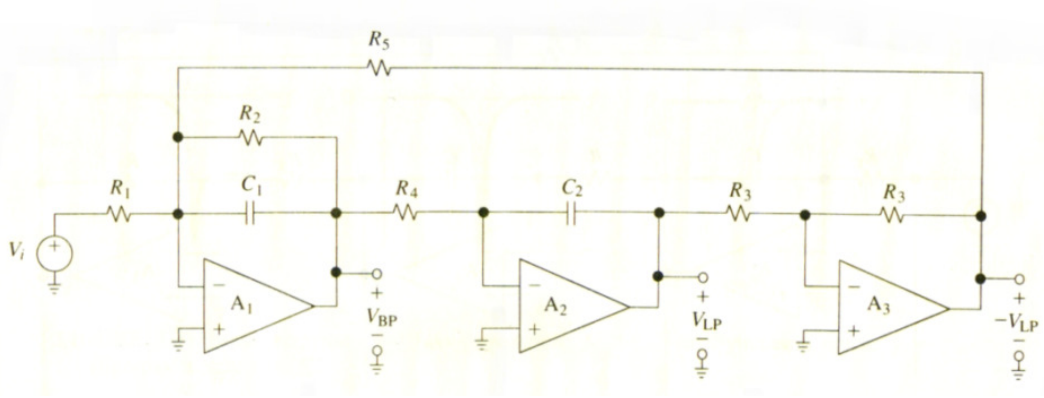


Figure 2.12 Active RC biquadratic filter circuit [1].

The voltage transfer function for the SC Tow Thomas Biquadratic filter is:

$$\frac{V_{Lp}(s)}{V_{in}(s)} = \frac{(C_1 \times \frac{f_C}{C_2})^2}{s^2 + s \times C_3 \times \frac{f_C}{C_2} + (C_1 \times \frac{f_C}{C_2})^2} \tag{2.17}$$

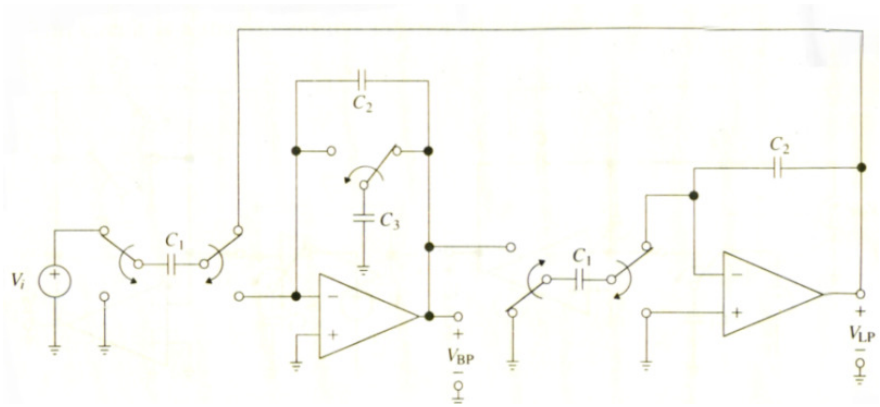


Figure 2.13 SC biquadratic filter circuit [1].

Until now, it was assumed that clock frequency f_{Clk} is much higher than the useful frequency range, so that charge flow by the switched capacitor can be considered as continuous. On the other hand, if the frequency of the signal is not negligible, comparing with f_{Clk} then the actual response will deviate from the ideal.

The deviation is illustrated in Figure 2.14 for the case of the non-inverting integrator. As shown in the figure, the SC circuit has similar behavior for a maximum frequency $f_0 = \frac{f_{Clk}}{10}$, where f_0 is the highest frequency component of the signal.

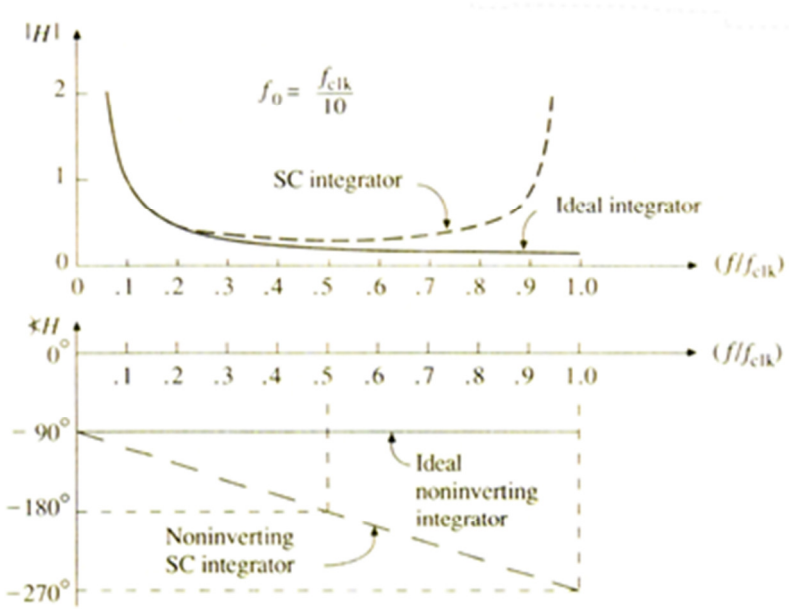


Figure 2.14 Non-inverting integrator magnitude and phase responses [1].

Assuming linear scales, the deviation of the SC integrator from ideality increases with frequency until f_0=f_{Clk}, the magnitude deviation becomes infinite and phase undergoes polarity reversal. These results are consistent with well-known sampled-data-principles, which state that the result of sampling a function of time at the rate of f_{Clk} samples per second is a replication of its frequency spectrum at integral multiples of f_{Clk}.

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2.2.2 CONTINUOUS TIME TECHNOLOGY

The OPAMP-RC active circuits and SC circuits are not suitable for wireless communication, for example, it is desired that the circuit be physically very small, work in frequencies on the order of tens to hundreds of MHz, consume low power and function in a low level signal and high noise environment. In addition, it is frequently necessary to include both the analog continuous-time and the digital signal processing devices on the

same semiconductor chip. Under these criteria, OPAMP-RC and SC techniques are no longer satisfactory.

The base of transconductance-C filters is the operational transconductance amplifier (OTA). An OTA is a voltage-controlled current source with infinite input and output impedances. OTAs are not usually implemented in bipolar form. Rather, they are often implemented using CMOS, BiCMOS, or GaAs technology.

With these technologies, resistors are impractical, because take up excessive areas to realize resistors of the resistance values usually necessary for these circuits. When a resistor is required, an equivalent resistance is realized by circuits using one or more OTAs. Therefore, a filter employs only OTAs and capacitors.

In the technologies used to fabricate OTA-C circuits, the absolute values of capacitors cannot be controlled with any acceptable degree of accuracy. Similar to SC filters, the circuit of a typical OTA-C filter can be made to depend only on the ratios of capacitances. These ratios can be controlled within a fraction of a percent.

An OTA is a differential-input, grounded output two port. The model with input and output impedance is shown in Figure 2.15.

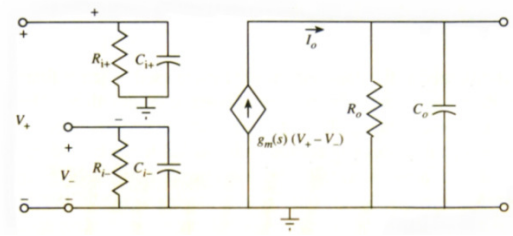


Figure 2.15 Model of an OTA with input and output impedances [2].

In an ideal OTA model, the input resistance approaches infinity and the output resistance approaches infinity. Figure 2.16 shows the ideal model of an OTA.

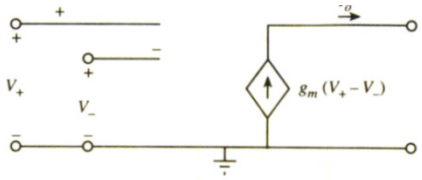


Figure 2.16 Ideal model of an OTA [2].

An idealized small-signal OTA is represented in the literature by the symbol shown in Figure 2.17. The ground symbol is frequently omitted, but it is always implied.

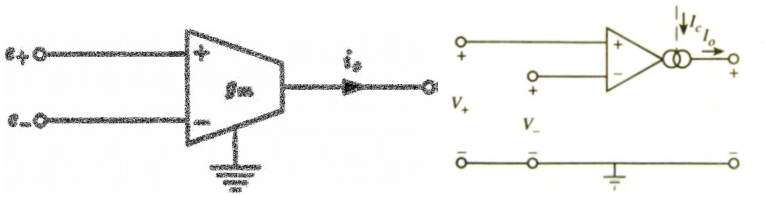


Figure 2.17 Typical symbols used to representation of an OTA [2,7].

An important application of an OTA is the simulation of grounded and floating resistors. Such circuits make possible the realization of large monolithic resistance values in a small chip area. An arrangement of a grounded resistor modeled by OTA circuit is shown in Figure 2.18a) and the equivalent resistor in Figure 2.18b). The output of the OTA is feedback to the negative terminal of input to prevent instability.

The value of the resistor is the following:

$$R_{eq} = \frac{1}{g_m} \tag{2.18}$$

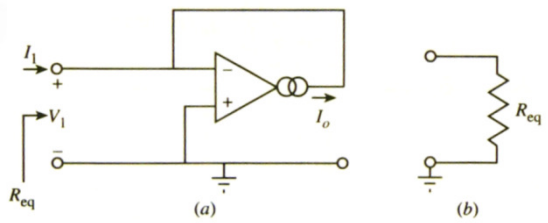


Figure 2.18 a) OTA gounded resitor circuit; b) Equivalent resistor [2].

To simulate a floating resistor, two OTAs are necessary. The arrangement of Figure 2.19a) shows the implementation circuit and Figure 2.19b) shows the equivalent resistor.

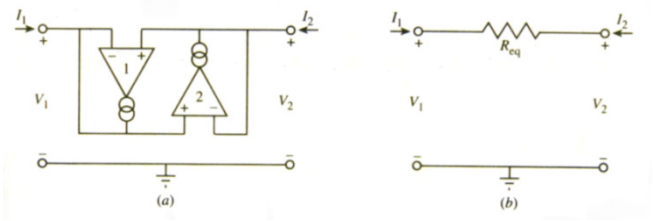


Figure 2.19 a) OTA floating resitor circuit; b) Equivalent resistor [2].

The circuit of Figure 2.20 realizes a lossless integrator. By grounding one of the input terminals, either an inverting or a noninverting integrator can be realized.

The transfer function is the following:

$$\frac{V_{0(s)}}{V^{+}(s) - V^{-}(s)} = \frac{g_m}{s \times C} \tag{2.19}$$

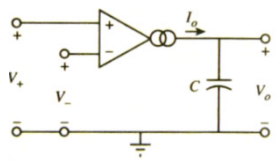


Figure 2.20 Integrator using OTA [2].

A general first-order OTA-C circuit is implemented as shown in Figure 2.21. The transfer function is:

$$\frac{V0(s)}{Vi(s)}=\frac{s\times C_1+g_{m1}}{s\times(C_1+C_2)+g_{m2}} \tag{2.20}$$

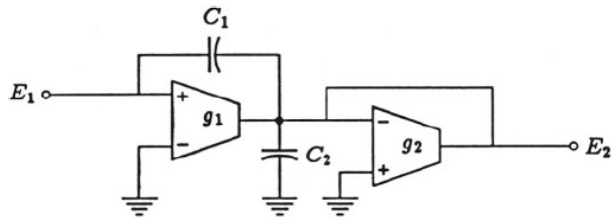


Figure 2.21 General first order OTA-C circuit [7].

Regarding second order biquadratic circuits, many of them have been developed along the last two decades using OTAs and capacitors. Similar to Opamp-RC biquad developments, many of these OTA-C biquads have their unique features. Some of them are simple. Others are easy to tune. Still others, are more suitable for IC fabrication.

The circuit on Figure 2.22 shows a second order low pass filter, that realises the following transfer function:

$$\frac{V0(s)}{Vi(s)}=\frac{(g_{m1}\times g_{m2})/(C_1\times C_2)}{S^2+s\times\left(\frac{g_{m3}}{C_2}\right)+\left(\frac{g_{m1}\times g_{m2}}{C_1\times C_2}\right)} \tag{2.21}$$

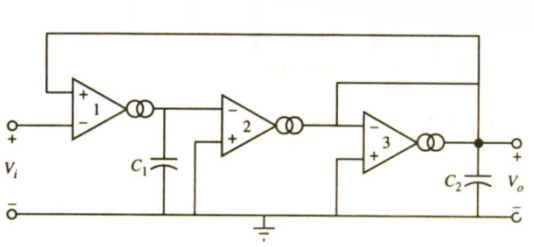


Figure 2.22 Second order OTA-C circuits [2].

As a practical observation, it should be noted that actual implementations of many of these circuits presented should have their input and feedback signals attenuated in order to maintain the OTA input voltages within the linear range of the device. The details as well as example circuits may be found in manufacturers data books.

2.3 IMPLEMENTATION OF FPAAS

The digital programmable FPGA or CPLD are commonly available and used, however the analog programmable circuits as the FPAA are considered a new branch. There are few vendors that deliver commercially FPAA circuits, while the number of academic projects on programmable analog circuits still growing.

2.3.1 ACADEMIC PROJECTS

Most devices encountered in scientific documents are academic projects. These devices are used for Research and Development (R&D). This chapter will put focus on two Research groups. The first one is the Cooperative Analog Digital Signal Processing (CADSP) group at Georgia Institute of Technology which develops a Continuous time FPAA, the RASP device. The second group mentioned, is a team of researchers from the University of Ulm and University of Freiburg which also developed a FPAA on continuous domain [10, 14].

RECONFIGURABLE ANALOG SIGNAL PROCESSOR (RASP)

The RASP is an FPAA designed by Tyson S. Hall in his Ph.D. thesis. Since then, it has been developed by the CADSP group at Georgia Institute of Technology. RASP 1.0 was fabricated in a 0.5 µm standard CMOS process. This FPAA contains two CABs connected by a floating gate crossbar switch network. The CAB design included a band pass filter module, 4 x 4 vector matrix multiplier, and three wide range OTAs.

The fundamental piece of technology for this reconfigurable system is the floating-gate-transistor. These are transistors whose gates are entirely surrounded by electrical insulator without DC path to ground, which allows stored charge to be retained. Floating gates have established themselves in digital circuits as a reliable non-volatile-memory storage, used in flash and EEPROM. An important feature of these devices is that they can be fabricated in a standard CMOS process. The layout for a floating gate is illustrated in Figure 2.23. The red poly 1 is the gate of this pFET. It has no direct contacts and is completely surrounded by oxide. This floating node is shown to have two voltage signals coupled onto it by capacitances, a tunneling voltage and an input voltage. A MOS capacitor is used for tunneling due to its high quality oxide and a poly capacitor is used for the input voltage.

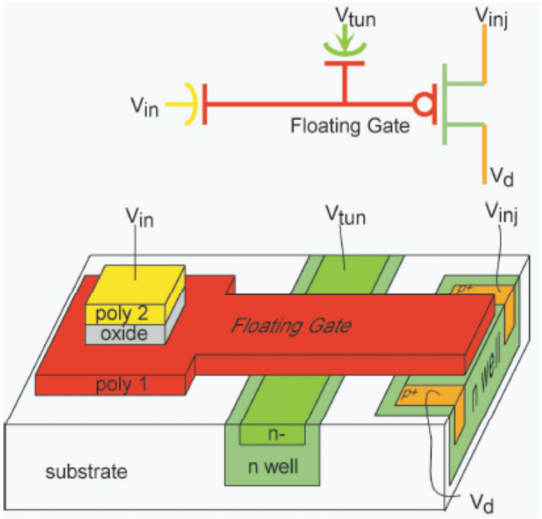


Figure 2.23 Floating gate transistor layout [9].

The RASP family of FPAAs has been developed by the CADSP research group over the last several years.

RASP 1.0 was designed as a test IC to study the floating gate switches and the interaction between the CAB components and the switch matrix. A two CAB system was sufficient to test the concept of floating-gate-transistor used in FPAAs. Each CAB has components critical to signal processing applications, including a 4 x 4 matrix vector multiplier, three wide range OTAs and a transistor only version of the auto-zeroing floating gate amplifier (AFGA). Two CAB architecture is shown in Figure 2.24, the input and output signals are routed to the rows of the switch matrix.

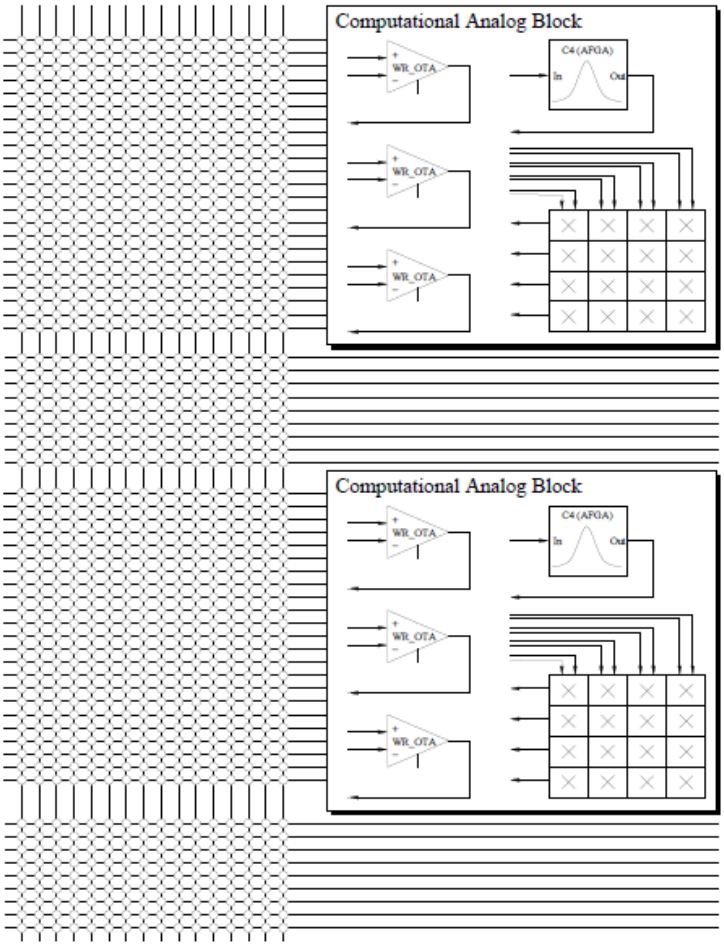


Figure 2.24 RASP 1.0, two Computational Analog Blocks (CABs) [8].

RASP 1.0 has one 16 x 64 crossbar switching matrix that provides local interconnects between the two CABs and connections to the external I/O signal lines. The switching matrix uses floating gate transistors as the switches.

RASP 1.5 is an FPAA that is similar in size to RASP 1.0, but it has a number of small circuit and architectural improvements that allow the system level functionality of the computational logic to be further tested. The RASP 1.5 FPAA was fabricated in 0.5 µm CMOS process. As shown in Figure 2.25, the routing infrastructure is achieved with a single, fully connectable crossbar switch. The switch network has 40 columns (drains) and 92 rows (sources). The inputs and outputs from all of the components in the two CABs connect to the rows of the switch network.

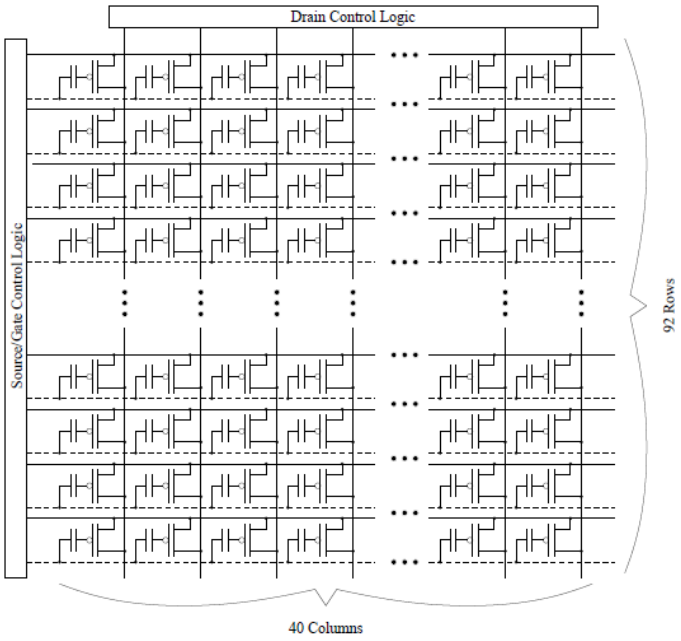


Figure 2.25 Crossbar switch matrix [8].

In RASP 1.5, there are two CABs with a single switch network connecting them together. Each CAB on RASP 1.5 contains a four-by-four matrix multiplier, three wide range OTAs, three fixed value capacitors, a coupled current conveyor (C4) second order section (SOS), a peak detector, a min detector, and two FET transistors. Figure 2.26 shows the described CAB components.

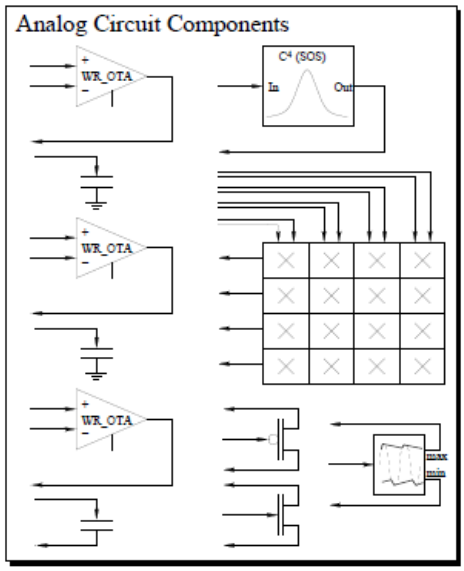


Figure 2.26 Computational analog block (CAB) [8].

Other RASP versions were developed as RASP 2.5 and RASP 2.7 in the period 2004 -2007. Newest versions, RASP 2.8 were developed on 2008 and RASP 2.9 developed in 2009.

Version RASP 2.8a is a general-purpose FPAA. It was fabricated in a 0.35 μ*m* double-poly CMOS process through Taiwan Semiconductor Manufacturing Corporation (TSMC) with a die size of 3 mm × 3 mm, it was able to accommodate 32 CABs. These CABs contain a variety of basic analog components such as: nFETs, pFETs, and capacitors, 9 OTAs, floating-gate input OTAs, MITEs and T-gates. In addition to the CAB components, there are fifty thousand floating-gate switches that can be used for computation. Advancement in this line of FPAA is the use of nearest-neighbor routing, which is an alternative to the existing horizontal/vertical routing, creates direct connections to the nearest CAB to the left, right, top and bottom. A system of bridge switches was also introduced. This allows for more lines to be drawn as locals and then bridged to the top and bottom local lines if needed. By using these shorter connections, the line capacitance is greatly reduced. Another advantage presented by the RASP 2.8a, and above, is the incorporation of on chip programming.

The RASP 2.9a general-purpose FPAA, is very similar to RASP 2.8a with the main difference being the size. The CABs and the routing are the same, but with a size of

5 mm × 5 mm, available space for 84 CABs. The extra CABs allow for larger systems to be implemented. Due to this chip largest size, it has a 200 pin package, so an adapter board was created to make it pin-compatible with the version 2.8 line. This adapter board lets it fit easily into the ZIF socket of the existing programming board. The main drawback of this is that the 108 I/O lines of the version 2.9 are reduced to the 52 I/O line of the version 2.8 (the amount that the current board can support). This has not been a problem because the 52 I/O has been more than enough to handle all of the systems implemented.

RASP 2.9b chip is identical to version 2.9a architecture and number of CABs, but to reduce the line delay, the routing was restricted to mostly local with the exception of four global lines per CAB stack column. This provides wires with less unnecessary length and thus less unnecessary capacitance. These design choices for this chip were made to decrease the capacitance and increase the signal bandwidth in an effort to target higher speed applications such as RF processing.

To program, communicate with, and test the RASP family of FPAAs the custom four-layer PCB in Figure 2.27 was built by CADSP group at Georgia Institute of Technology. This evaluation board communicates over and is fully powered by USB, but it has the capability to be powered by a 5V DC supply and communicate over a serial connection.

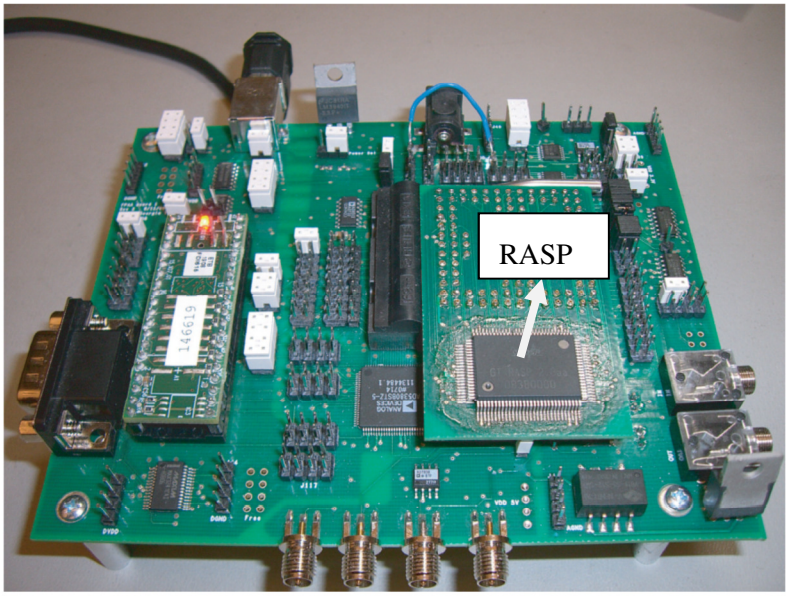


Figure 2.27 Evaluation board built by CADSP [9].

The board is controlled by an ATMEL ARM microcontroller for handling instructions from the computer using MATLAB commands. It also includes a 40 channel 14-bit DAC, a 4-channel 8-bit ADC, audio input/output amplifiers and jacks, and all of the programming circuitry not already on-chip.

FPAA BY UNIVERSITY OF FREIBURG, DEPARTMENT OF MICROSYSTEMS ENGINEERING (IMTEK)

A team of researchers, Joachim Becker and Yianos Manoli from the University of Ulm and University of Freiburg presented an FPAA built on continuous-time technology in technology CMOS of 0,13 µm. The device has OTAs and capacitances. It has a hexagonal lattice CAB layout.

Figure 2.28a) illustrates the layout of an array with 7 CABs, which features 6 inputs and one fully enclosed CAB. Figure 2.28b) shows the single CAB design.

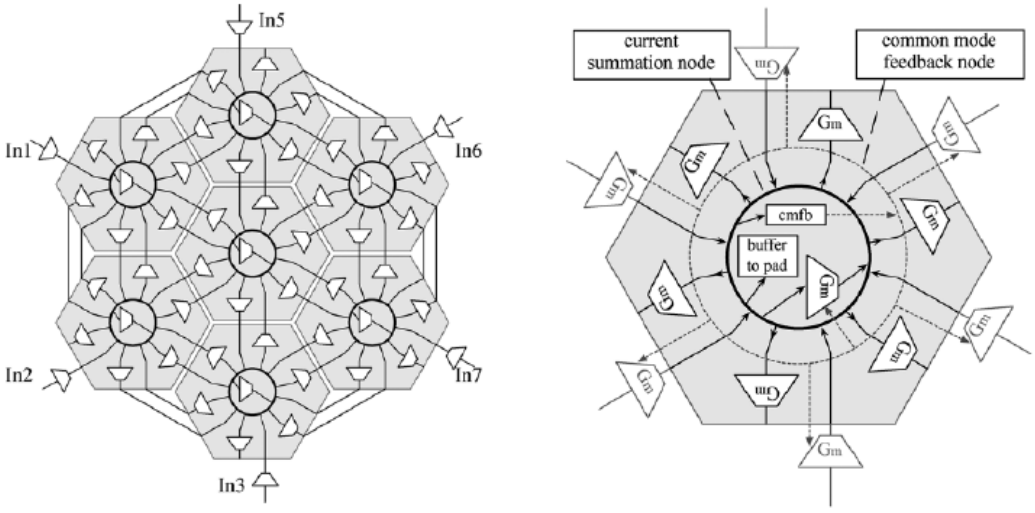


Figure 2.28 a) FPAA topology with 7 CABs; b) Diagram of a CAB [14, 15].

Due to the high demands in time and cost of integrated circuit design, rapid-prototyping has become an important field of microelectronics.

The laboratory for microelectronics at the department of microsystems engineering (IMTEK) at the university of Freiburg, Germany, develops field FPAAs for reconfigurable instancing of continuous-time high-frequency filters.

In the latest FPAA chip, it has 55 tunable Gm-cells arranged in a hexagonal grid. Through this special topology, it is possible to enable reconfigurable signal routing without switches in the signal path by switching the power supplies of the Gm-cells and provide all connectivity necessary for all orders of feedback needed for the filters. The latest report on this work states the Gain-Bandwidth product is 186 MHz [16].

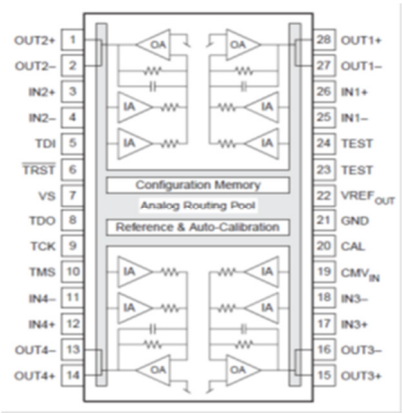
2.3.2 COMMERCIAL PROJECTS

There are several families of programmable analog circuits commercially available. They differ in principle of operation, resources and area of application. On this section is mentioned several FPAAs available on the market since last decade. Some of them already discontinued.

ISPPAC FAMILY FROM LATTICE SEMICONDUCTOR

The ispPAC family devices work according to CT principle and can be programmed in-system. The circuits have different functionalities.

The ispPAC10 In-System Programmable (ISP) analog circuit is digitally configured via nonvolatile E2CMOS technology. The analog function modules, called PACblocks, replace traditional analog components such as OPAMPs and active filters, eliminating the need for most external resistors and capacitors. With no requirement for external configuration components, ispPAC10 expedites the design process, simplifying prototype circuit implementation and configuration while providing high performance and integrated functionality. Figure 2.29 shows the functional block diagram with the four instrumentation amplifiers blocks and device main features.

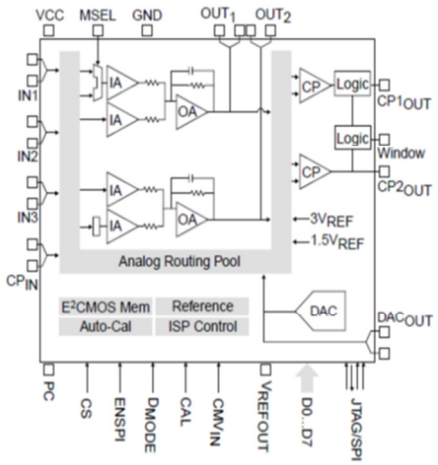


Main characteristics:

- Four Instrument amplifier gain / attenuation stages.
- Available four inputs and outputs.
- Precision active filtering,10 kHz to 100 kHz.
- No external components needed for configuration.
- Nonvolatile E2CMOS cells.
- IEEE 1149.1 JTAG serial port programming.

Figure 2.29 Functional block diagram ispPAC10 [17].

The ispPAC20 is an ISP analog circuit, digitally configured via nonvolatile E2CMOS technology; it includes an 8-bit DAC and dual comparators with no requirement for external configuration components. Figure 2.30 shows the functional block and device main features.



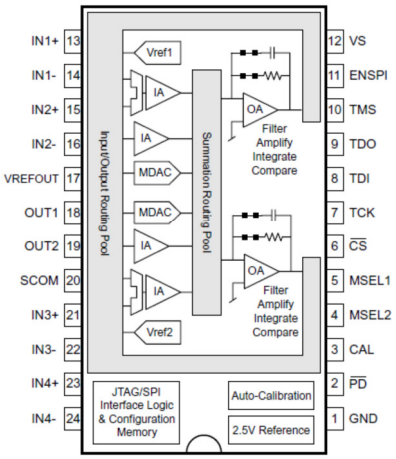
Main characteristics:

- Two instrument amplifier gain / attenuation stages.
- Three input signals.
- Precision active filtering, 10 kHz to 100 kHz.
- 8 bit DAC and fast dual comparator.
- Nonvolatile E2CMOS cells.
- IEEE 1149.1 JTAG serial port programming.

Figure 2.30 Functional block diagram ispPAC20 [18].

The ispPAC30 is digitally configured via SRAM and utilizes E2CMOS memory for non-volatile storage of its configuration. The flexibility of ISP enables programming, verification and unlimited reconfiguration. The ispPAC30 is a complete front end solution

for data acquisition applications using 10 to 12 bit ADCs. It provides multiple single-ended or differential signal inputs, multiplexing, precision gain, offset adjustment, filtering, and comparison functionality. It also has complete rout ability of inputs or outputs to any input cell and then from any input cell to either summing node of the two output amplifiers. Figure 2.31 shows the functional block diagram and main features.

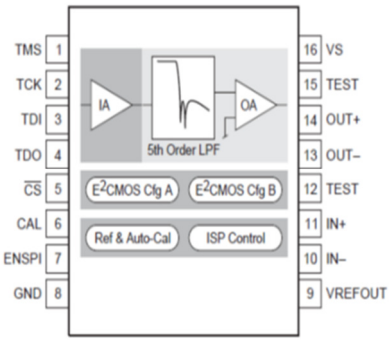


Main characteristics:

- Flexible interface and programming control.
- Full configuration capability, SPI or JTAG modes.
- Unlimited device updates using SRAM register.
- E2CMOS for non-volatile configuration storage.
- Real-time microcontroller configuration /control.
- Amplifier, filter, integrator or comparator modes.
- 7 filter frequencies (50 kHz to 600 kHz)

Figure 2.31 Functional block diagram ispPAC30 [19].

The Device ispPAC80/81 is a programmable 5th order CT active filter. The filter type configuration could be Butterworth, Chebychev, Legendre, Elliptic, Linear Phase and Bessel. Also, the gain and corner frequency can be configured. Figure 2.32 shows the functional block diagram and main features of device.



Main characteristics:

- Instrument amplifier gain stage.
- CT fifth order low pass topology.
- Dual, A/B configuration memory.
- Nonvolatile E2CMOS cells.
- IEEE 1149.1 JTAG serial port programming.

Figure 2.32 Functional block diagram ispPAC80/81 [20,21].

The ispPAC10, ispPAC20, ispPAC30, and ispPAC80/81 devices are mature products which were discontinued in 2007. These devices are no longer available from Lattice and there are no direct replacement products available for these devices from the manufacturer.

PSOC FAMILY FROM CYPRESS SEMICONDUCTOR

The programmable embedded system-on-chip (PSoc) integrates configurable analog and digital peripheral functions, memory and a microcontroller on a single integrated circuit. The Cypress PSoc architecture consists of configurable analog and digital blocks, a CPU subsystem and programmable routing interconnection between PSoc blocks. Figure 2.33 shows the device roadmap for the PSoc family.

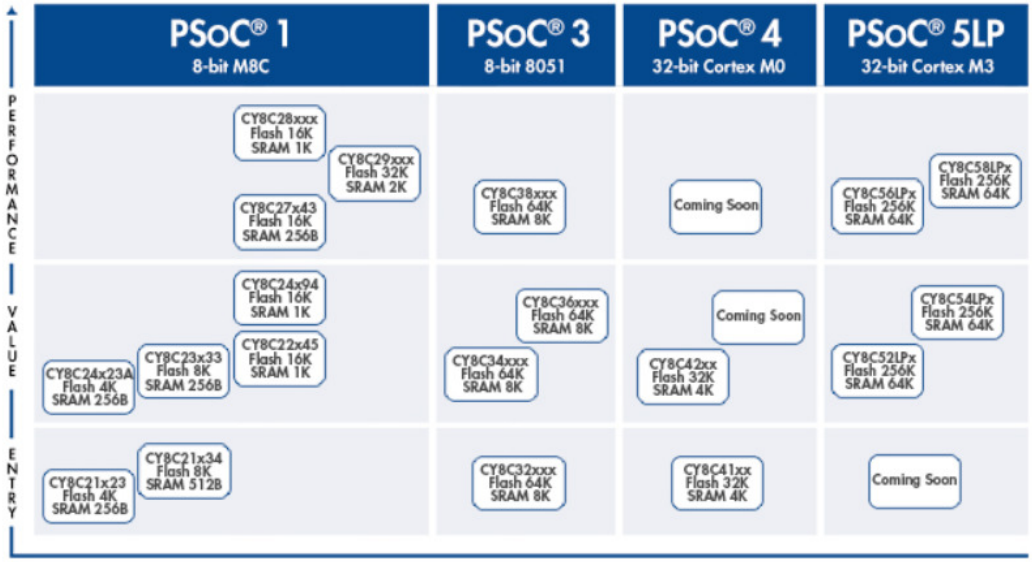


Figure 2.33 Cypress PSoc device roadmap.

PSoc 1 is the world's first Programmable embedded System-on-Chip integrating configurable analog and digital peripheral functions, memory, and a microcontroller on a single chip. Powered by Cypress's proprietary 8 bit M8C core, the PSoc 1 portfolio of devices provides the system designer analog integration, flexible I/O routing and control of power consumption. Figure 2.34 shows the architecture of IC.

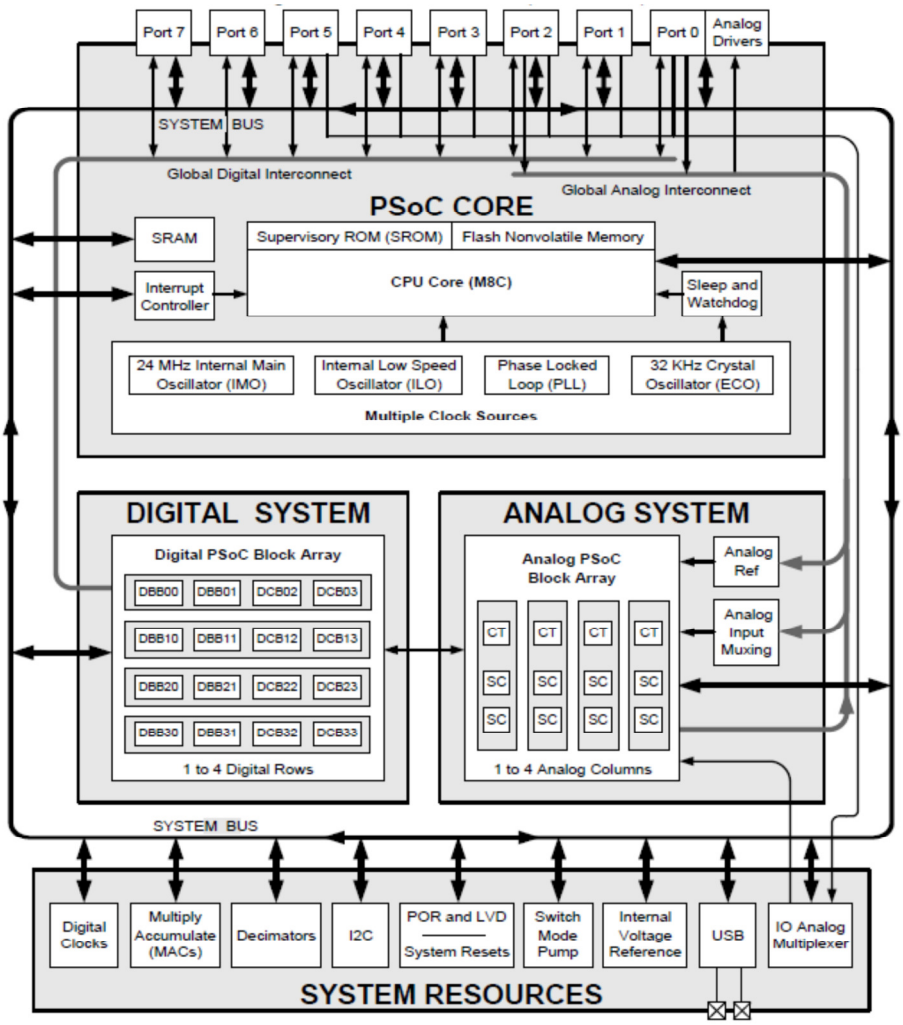


Figure 2.34 Cypress PSoc 1 device functional block diagram [22].

The analog subsystem of PSoc 1 is composed of analog blocks arranged in a column configuration. These analog blocks are either CT blocks or SC switch blocks.

The CT blocks are programmable analog blocks that can be configured as comparators or programmable gain amplifiers (PGAs). These blocks are built around low-noise and low-offset OPAMPs. The large number of analog multiplexers in the CT block provides high configurability. The SC Blocks are also built around low-noise, low-offset OPAMPs surrounded by analog multiplexers. These blocks are unique because groups of capacitors and switches surround the OPAMPs and multiplexers.

PSoc 3 has a CPU and memory subsystem, digital subsystem, an analog subsystem and system resources. Figure 2.35 shows the block diagram.

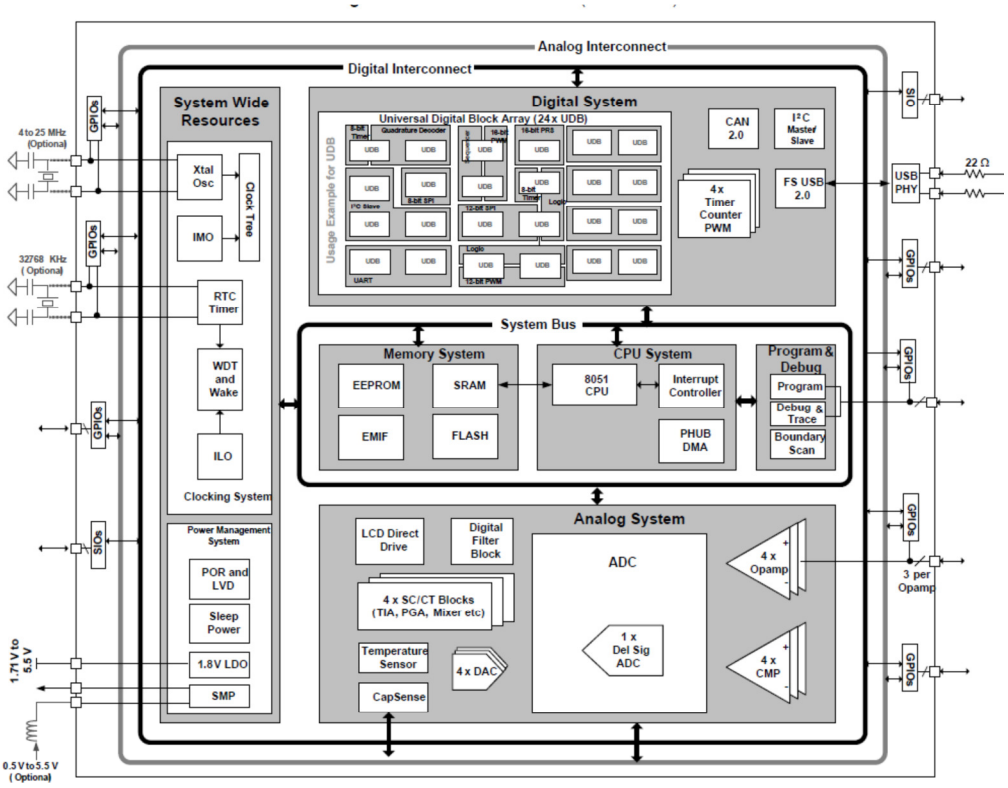


Figure 2.35 Cypress PSoc3 device functional block diagram [23].

PSoc 4 is a true programmable embedded system-on-chip, integrating custom analog and digital peripheral functions, memory, and an ARM Cortex-M0 microcontroller on a single chip.

This type of system is different from most mixed-signal embedded systems, which use a combination of a microcontroller unit (MCU) and external analog and digital peripherals. Figure 2.36 shows the architecture of IC.

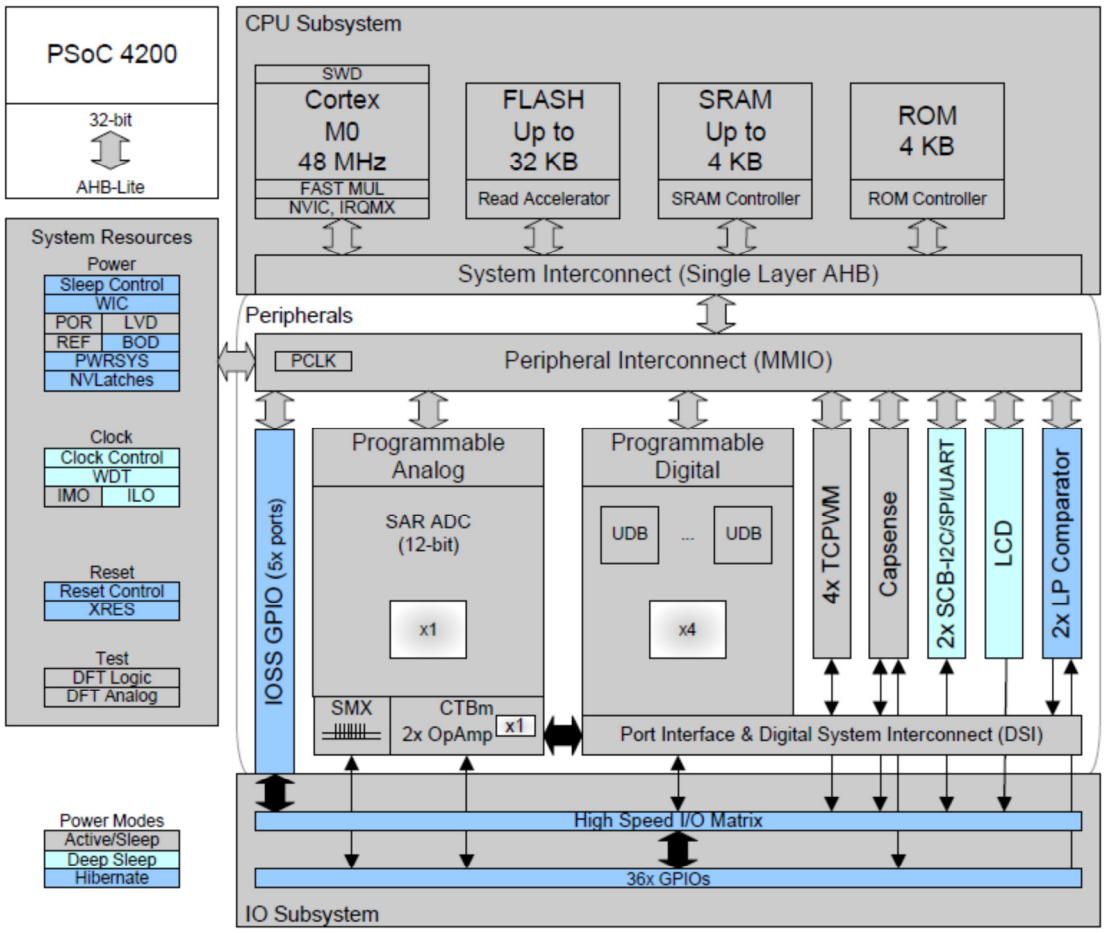


Figure 2.36 Cypress PSoc4 device functional block diagram [25].

PSoc 4 provides an analog system that includes a fast 12-bit successive approximation register analog-to-digital converter (SAR ADC) and a CT Block mini (CTBm). PSoc 4100 and PSoc 4200 devices have a CTBm block which consists of two programmable OPAMPs and a switch matrix.

PSoc 5LP is a true programmable embedded system-on-chip, integrating configurable analog and digital peripherals, memory, and a microcontroller on a single chip. Figure 2.37 shows the block diagram.

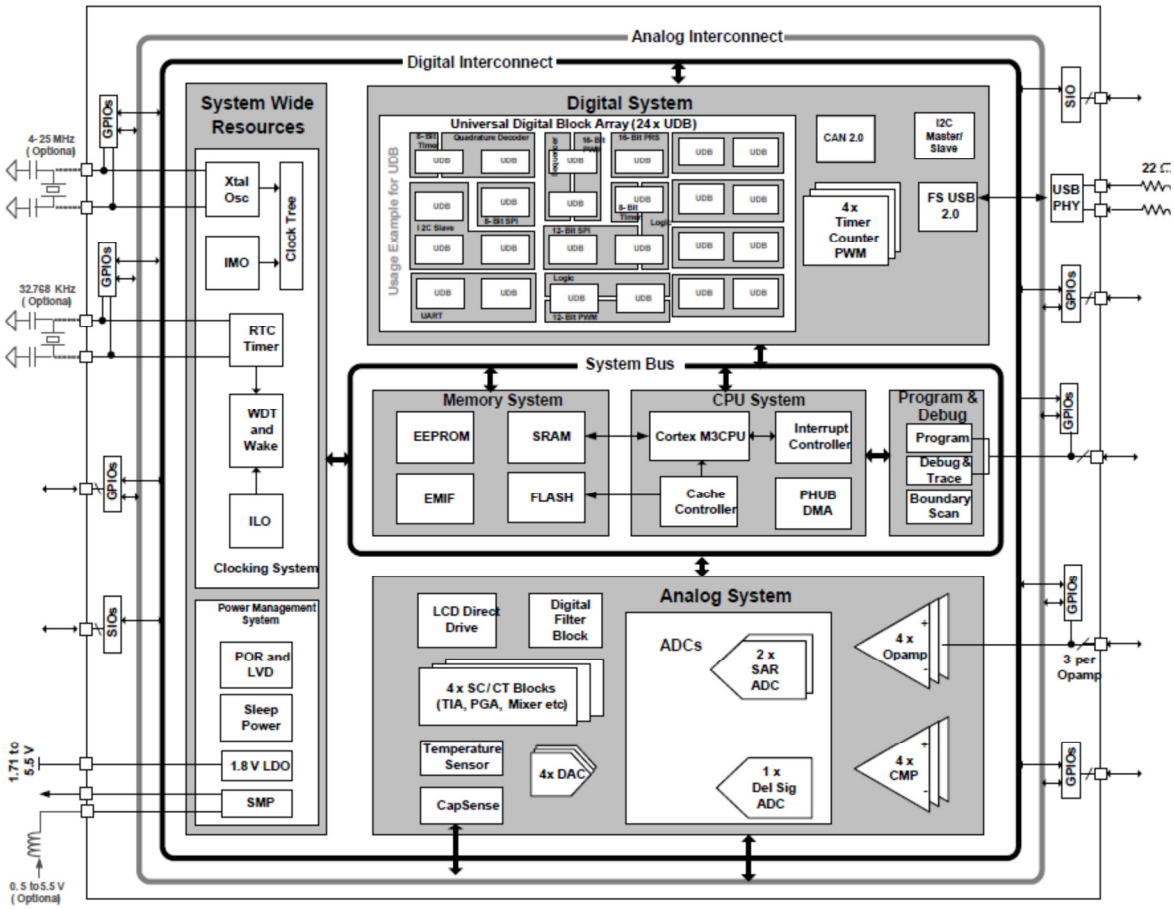


Figure 2.37 Cypress PSoc 5LP device functional block diagram [26].

The analog programmable system creates application specific combinations of standard and advanced analog signal processing blocks. These blocks are interconnected to each other and also to any pin on the device, providing a high level of design flexibility. The features of the analog subsystem include:

- Flexible, configurable analog routing architecture provided by analog globals, analog mux bus, and analog local buses.
- High resolution Delta-Sigma ADC.
- Two successive approximation (SAR) ADCs.
- Four 8-bit DACs that provide either voltage or current output.
- Four comparators with optional connection to configurable LUT outputs.

- Four configurable SC/CT blocks for functions that include OPAMP, unity gain buffer, programmable gain amplifier, trans-impedance amplifier and mixer.
- Four OPAMPs for internal use and connection to GPIO that can be used as high current output buffers.
- Precision reference for generating an accurate analog voltage for internal analog blocks.

FPAAS AND DPASPS FROM ANADIGM SEMICONDUCTOR

Anadigm has a full range of 5 V and 3.3 V programmable analog arrays. They are divided into static programmable devices (FPAA), which require a reset before loading. A new configuration bit stream and so called dynamically programmable Analog Signal Processors (dpASP) provides real time dynamic reconfigurability that allows the functionality of the dpASPs to be reconfigured in-system by the designer or "on-the-fly" by a microcontroller/processor.

A dpASP can be programmed to implement multiple analog functions and/or adapt as mentioned above "on-the-fly" to maintain precise operation required by applications that have changing requirements in real time, such as signal conditioning, filtering, data acquisition and closed-loop control.

The first FPAA from Anadigm was marked AN10E40 and contained twenty configurable analog blocks. It belongs to the first generation of FPAA circuits, but is not already available.

Anadigm offered a second generation family of FPAA called AnadigmVortex. It is powered from a 5 V supply. The Vortex family contains eight circuits and the most popular of them is the device AN221E04. This generation is discontinued because Anadigm ability to manufacture this product was ceased due to the obsolescence of the wafer fabrication process by the subcontractor later in 2014.

The third generation, AnadigmApex family is a successor of AnadigmVortex with the commonly used AN231E04 circuit. One of the most important differences between the

third and second generation families is the supply voltage. The third generation family is powered from a 3.3 V supply instead of 5 V. This results in easy interfacing with contemporary 3.3 V microcontrollers with no need of using level-shifters.

Two members of the AnadigmApex family are currently providing access to the latest technology in programmable analog devices, the FPAA AN131E04 and dpASP AN231E04. Both of these devices provide seven analog I/O Cells and four Configurable Analog Blocks (CABs).

Figure 2.38 shows the roadmap history of Anadigm devices since the spinoff from Motorola.

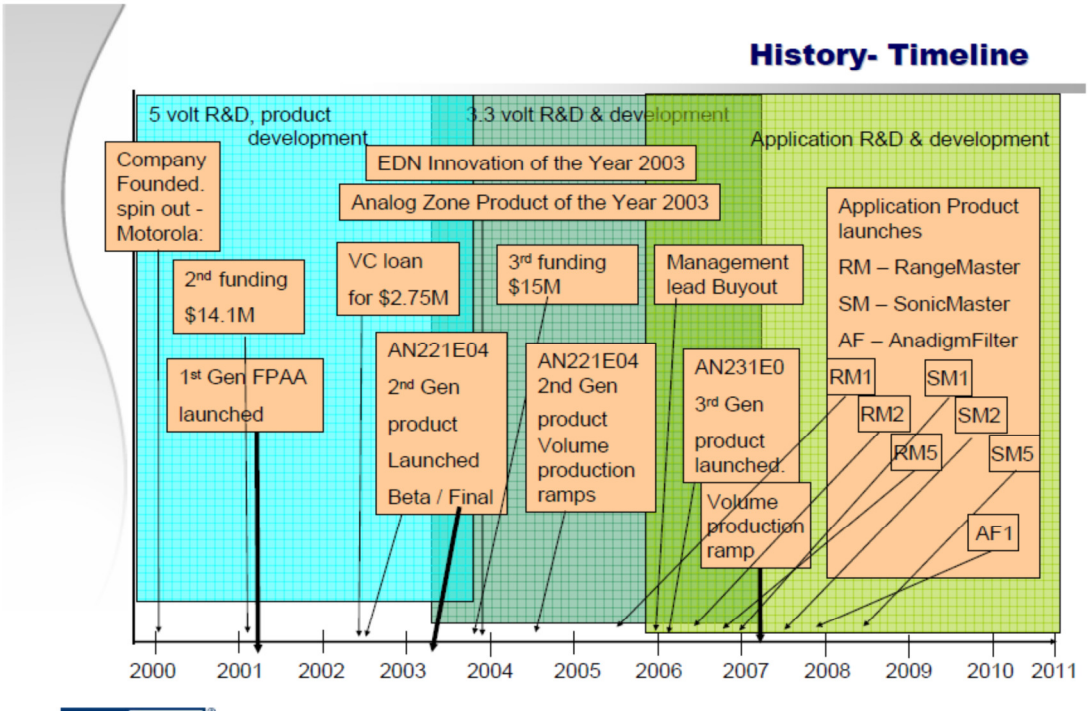


Figure 2.38 Anadigm device history since Spinoff from Motorola [28].

As the first and second generations were discontinued by Anadigm, the next chapter will be focus on the third generation of FPAA/dpASP, AnadigmApex as these devices are the core for the hardware implementation on this Thesis.

2.4 FPAA/DPASPS FROM ANADIGM (ANADIGMAPEX)

The AnadigmApex represents the third generation of FPAA/dpASP devices from Anadigm. Two members of the AnadigmApex family are AN131E04 and AN231E04. Both of these devices provide 7 analog I/O Cells and 4 Configurable Analog Blocks (CABs).

This third generation delivers improved analog performance. The configuration interface of the AN23x devices is enhanced to accommodate dynamic reconfiguration, a capability that allows analog circuit functionality to be controlled by a host processor.

2.4.1 ARCHITECTURE OVERVIEW

The device processes analog signals in their I/O Cells and CABs. These structures are constructed from a combination of conventional SC circuit elements and are programmed from off-chip non-volatile memory or by a host processor. The SRAM based AN23x devices are dynamically reconfigurable and behavior of this dpASP can be modified partially or completely while operating. Dynamic reconfiguration allows a companion host processor to send new configuration data to the dpASP while the old configuration is running. Once the new data load completes, the transfer to the new analog signal processing configuration happens in a single clock cycle and allows the development of analog systems that can be updated on-the-fly.

The AN13x devices are also SRAM based and also can be reprogrammed as many times as desired, however the device must always first be reset before get a configuration data set. Figure 2.39 shows the block diagram of device.

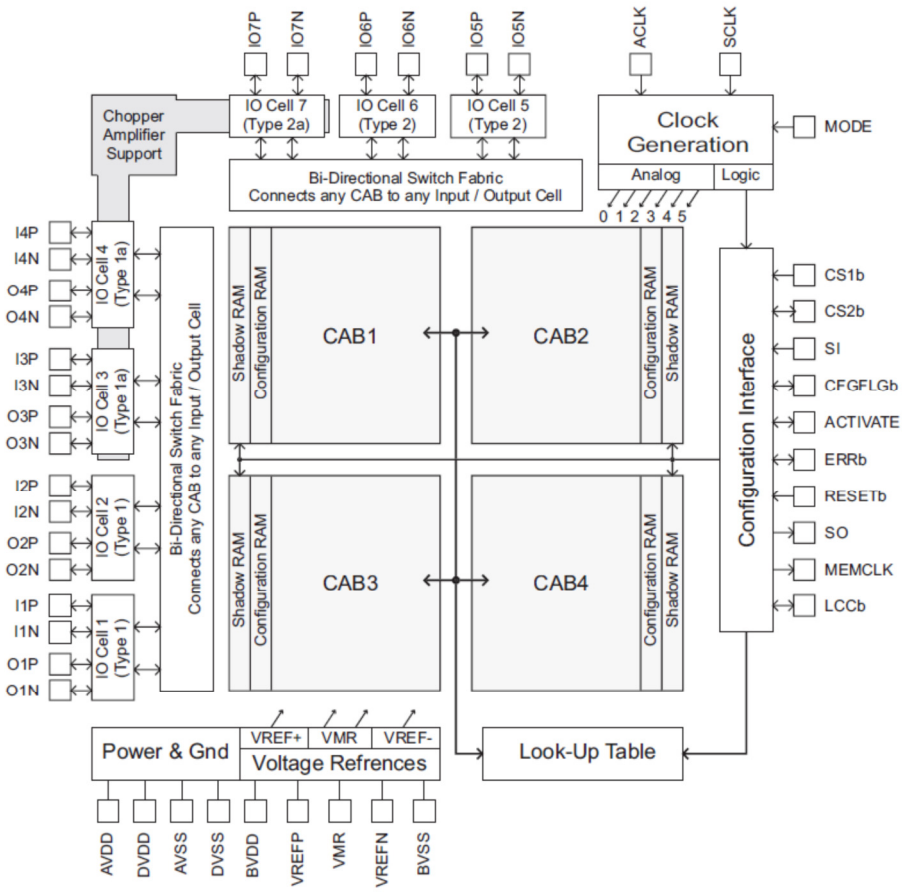


Figure 2.39 FPAA AN13x and dpASP AN23x block diagram [27].

Most of the analog signal processing occurs within the CABs and is done with fully differential switched capacitor circuitry.

The CABs share access to a single Look Up Table (LUT) which offers a method of adjusting any programmable element within the device in response to a signal or time base. The LUT can also be used to implement arbitrary input-to-output transfer functions as the case of sensor linearization, generate arbitrary signals and construct voltage dependent filtering.

A voltage reference generator supplies reference voltages to each of the CABs within the device and has external pins for the connection of filtering capacitors.

Analog signals are routed in and out of the device core via the available I/O cells as follows:

- Two I/O type 1.
- Two I/O type 1a.
- Two I/O type 2.
- One I/O type 2a.

Type 1 and type 1a IO cells contain both passive and active circuitry which allows direct signal input and output, building of active filters, sample and hold circuits, digital inputs, and digital outputs. The response of continuous time input and output filters is determined by a combination of internal programming and external components. Figure 2.40 shows the available options.

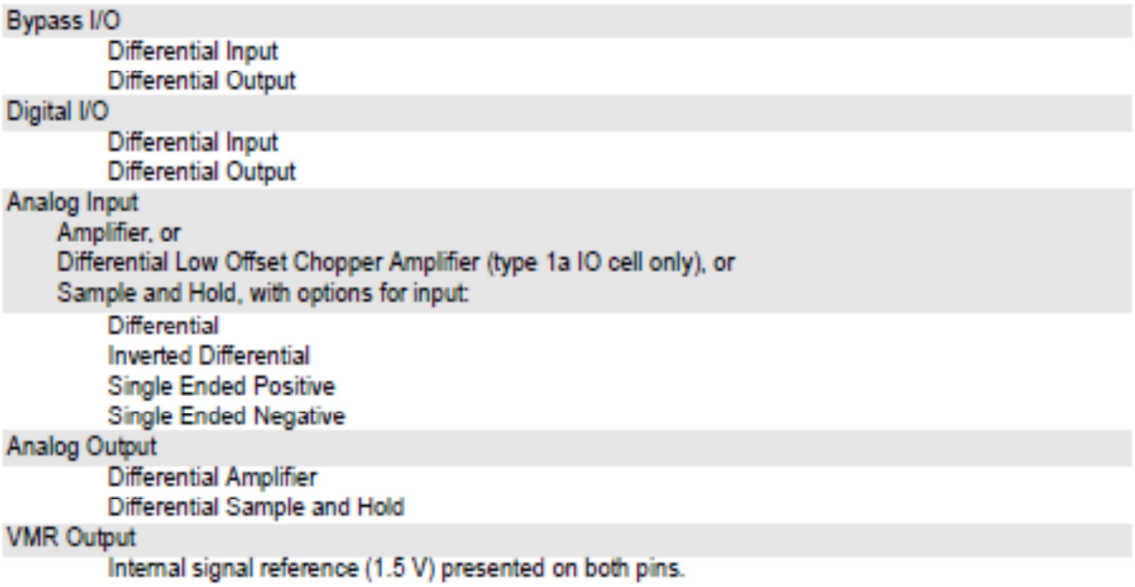


Figure 2.40 Types 1 and 1a I/O cell options [27].

Type 2 and type 2a IO cells are simpler and can implement direct input and output, reference voltage output, digital input, and digital output. Figure 2.41 shows the available options.

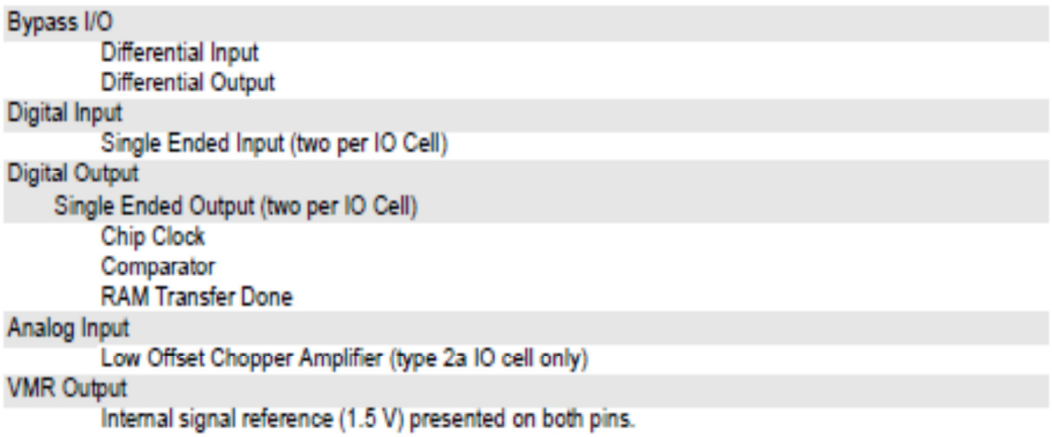


Figure 2.41 Types 2 and 2a IO cell options [27].

Any one of the type 1a or type 2a IO cells can have access to a specialized chopper amplifier resource which allows accurate amplification of very low energy input signals.

2.4.2 CONFIGURATION INTERFACE CONNECTIONS

The behavior of the analog signal processing circuits within AN13x/AN23x devices is dictated by the contents of its volatile SRAM configuration memory. At power-on-reset, the dpASP/FPAA clears its memory, placing the device in a beginning condition. Once this power-on-reset sequence concludes, the device is ready to accept configuration data. The first configuration data set loaded into the device after a reset is called a primary configuration.

AN13x devices accept only primary configurations. A reset is required before reconfiguring an AN13x device. AN23X devices on the other hand can be reconfigured without reset.

The configuration interface presents itself as either a serial data master or serial data slave. As a serial data master, the FPAA/dpASP can automatically retrieve its configuration data set from any industry standard SPI PROM attached. As a serial data

slave, the FPAA/dpASP is compatible with SPI signaling from a host processor and can accept its configuration data from that host.

DYNAMIC OPERATION

In dynamic operation, a companion host processor sends configuration data to the dpASP/FPAA using SPI compatible signaling. The change may be as simple as a minor adjustment of a gain or corner frequency or involve a transformation of behavior, for instance from a transmitter to a receiver configuration. Figure 2.42 shows the configuration.

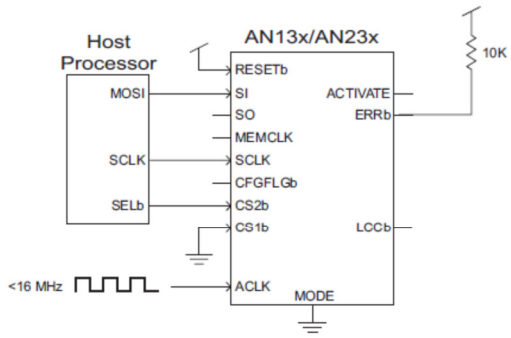


Figure 2.42 Configuration of single dpASP from a host processor [27].

Out of power-on-reset, the dpASP/FPAA remains in a beginning state, waiting for a configuration sequence. In order to configure, the host processor drives CS2b low then streams a configuration data set out of its serial data port. Normally, the dpASP will enable analog signal processing automatically at the conclusion of configuration.

Configuring of several dpASP/FPAA from a host processor is a matter of busing the serial clock and data signals to each of the devices. Figure 2.45 shows the parallel connection of the hosts MOSI, SCLK and select signals to an arbitrary number of dpASPs.

The LCCb pin of the upstream device is tied to the CS1b pin of the downstream device, holding off downstream configurations until the upstream device gets its configuration. This connection coupled with CFGFLGb pin behavior and logical

addressing enables the specific device select outputs. Entire chain of FPAA/dpASPs only requires a single select pin from the host.

ACTIVATE and ERRb nodes are tied together in order to facilitate the concurrent activation of analog circuitry and provide configuration error handling. When connecting two or more dpASPs together, as shown on Figure 2.43, it is important to connect together the CFGFLGb pins.

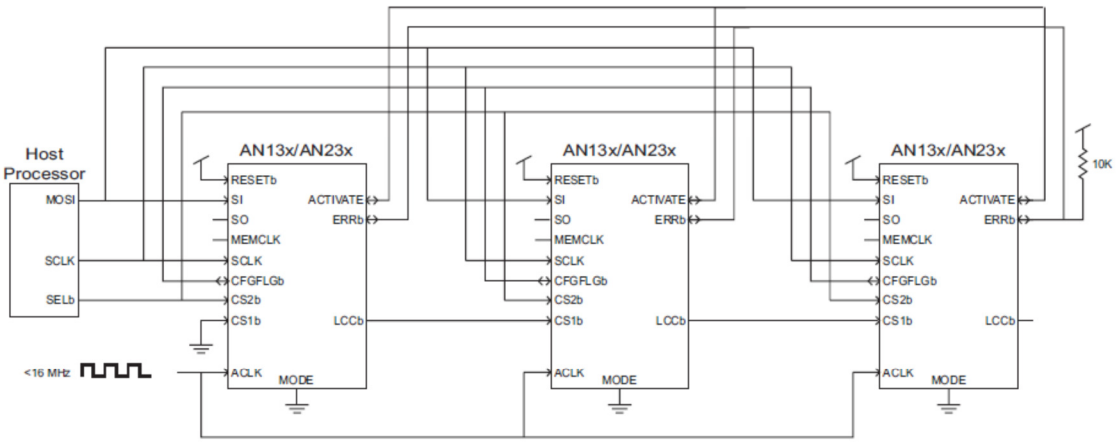


Figure 2.43 Configuration of multiple dpASPs from a host processor [27].

In fact, dynamic operation is the most powerful use model of Anadigm devices. The dpASP/FPAA is used with MODE tied low and consequently the configuration interface presents itself as a SPI compatible slave. The host processor can be used to simply manage the configuration tasks, downloading data to the dpASPs/FPAAs from its SPI master port. The real potential of programmable analog is much better when the host processor is also used to generate and download new configuration data sets on-the-fly as analog signal processing requirements change. This dynamic reconfiguration is only available on dpASP AN23x devices and is not available for FPAA AN13x device.

STATIC OPERATION

In static operation, the dpASP/FPAA will automatically read in its configuration data from an SPI PROM after a manual reset or on power-up. Figure 2.44 shows the configuration.

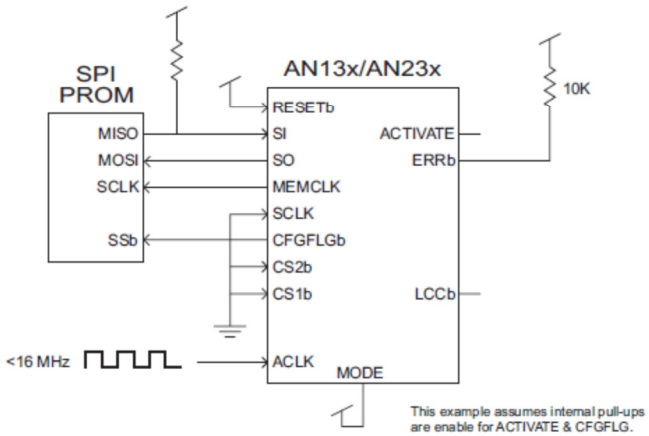


Figure 2.44 Single FPAA/dpASP, self-configuring from a SPI PROM [27].

At the conclusion of the power-on-reset sequence, CFGFLGb will be low, selecting the attached SPI PROM. The standard "read" command will be issued out of SO (clocked by MEMCLK). As MEMCLK continues, the SPI PROM responds with a serial data stream. This serial data stream is read by the SI pin. Normally, the FPAA/dpASP will enable analog signal processing automatically at the conclusion of configuration.

In this simplest use model, the FPAA/dpASP automatically detects power-on, resets itself, reads in configuration data from a standard SPI PROM, and begins analog signal processing. A subsequent reset or power cycle will cause the sequence to repeat.

A more advanced application of static configuration allows the connection of several FPAA/dpASPs to a single SPI PROM. In this scenario, the devices are daisy chained, the upstream (closer to the PROM) device's Local Configuration Complete (LCCb) pin feeds the downstream devices CS1b enable pin. The SPI PROMs MISO data output pin is

connected to all SI pins from FPAA/dpASPs. Also, all devices have their ACTIVATE and ERRb pins connected.

As with the single FPAA/dpASP example, the first device in the chain still provide the “read” command to the SPI PROM but provides the necessary clocking for *all* the serial configuration data. As the configuration completes for an *upstream* device, its LCCb asserts low and enables the next device in the chain (*downstream)* to receive its data.

ACTIVATE is an open-drain bidirectional pin. During configuration the ACTIVATE pin is asserted low. Analog circuitry is not enabled (activated) until the ACTIVATE pin moves to a high state. As the local configuration completes, the dpASP de-asserts its ACTIVATE pin and monitors the ACTIVATE node. The daisy chained LCCb to CS1b sequence continues until all dpASPs in the chain have received configuration data. At that point all of the dpASPs will have de-asserted ACTIVATE. Tying the ACTIVATE pin of all the devices in the configuration chain together ensures that analog signal processing does not begin in any of the devices until all of them have received their configuration data. Figure 2.45 shows the multiple chip connection.

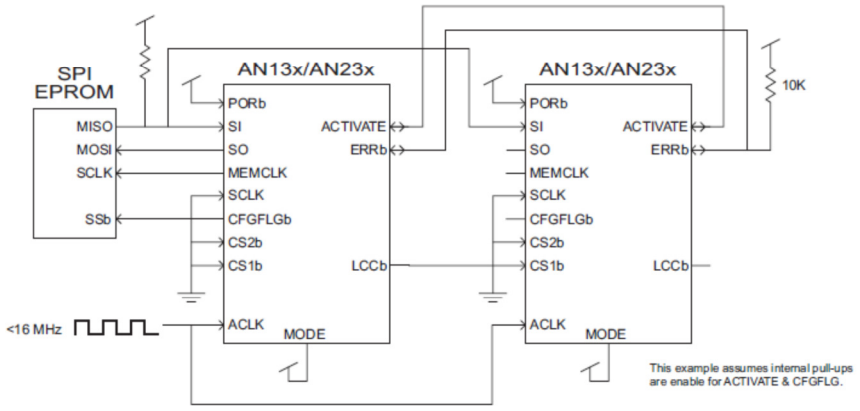


Figure 2.45 Multiple dpASPs, self-configuration from a single SPI PROM [27].

ERRb is also an open-drain bidirectional pin. The ERRb pin will assert low if illegal or corrupted data is detected. Tying the ERRb pin of all the devices in the configuration chain together ensures that if any device detects an error, then all of the devices in the chain will reset (including the SPI PROM) and the configuration sequence will re-start automatically.

2.4.3 CONFIGURABLE ANALOG BLOCK (CAB)

Most analog signal processing occurs in the Configurable Analog Block (CAB). Signal processing is accomplished using an architecture based on SC circuit design. Every CAB contains two OPAMPS, a comparator, banks of programmable capacitors, and a configurable routing and clock resources. Figure 2.46 shows the functional block diagram of a CAB.

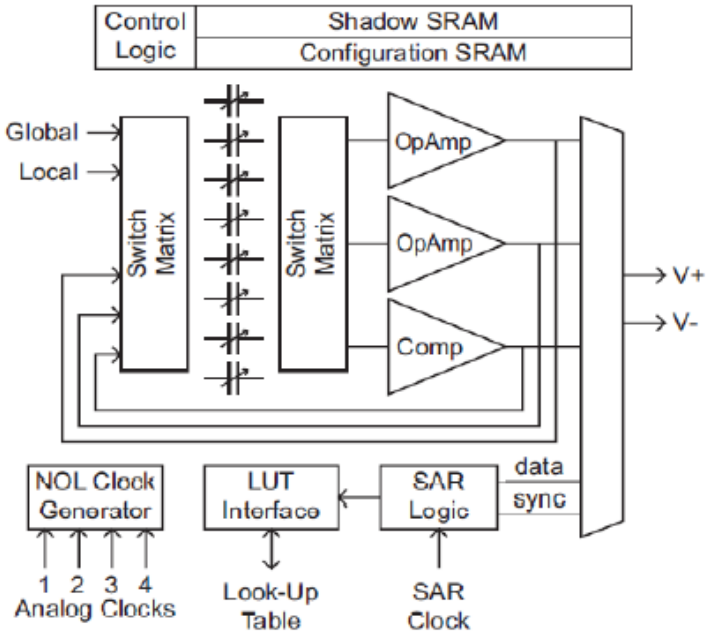


Figure 2.46 Block diagram of a CAB [33].

With SC signal processing, the absolute value of the components integrated into the chip is not important, but rather it is the ratio of the programmable capacitors employed and the clock frequencies that determine circuit response; both of which are well controlled. In order to further improve signal fidelity, all signal processing within the CABs is fully differential.

2.4.4 ANALOG AND CONFIGURATION CLOCK GENERATION

All signal processing clocks within the device are derived from the analog master clock signal presented on the ACLK pin. The ACLK signal gets split and divided down into two system base clocks (SYS1 and SYS2), the divisor being between 1 and 510. These two system clocks are further divided down into six additional clock domains: Clock 0 through Clock 5. Each of these 6 analog processing clocks can use either SYS1 or SYS2 as its base, and will further divide that base clock down by 1 up to 510. Figure 2.47 shows the clock block diagram.

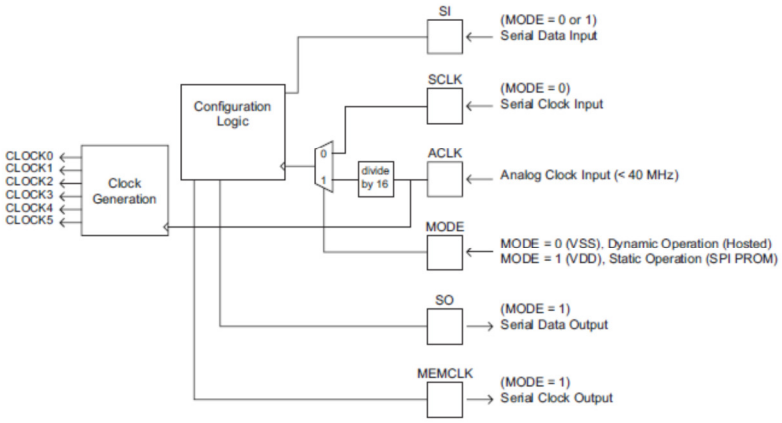


Figure 2.47 Clock control block diagram [27].

Figure 2.48 shows the clock settings for the dpASP AN231E04 by default in the program Anadigm designer 2. All clock signals could be parameterized using source clock base signals SYS1 or SYS2.

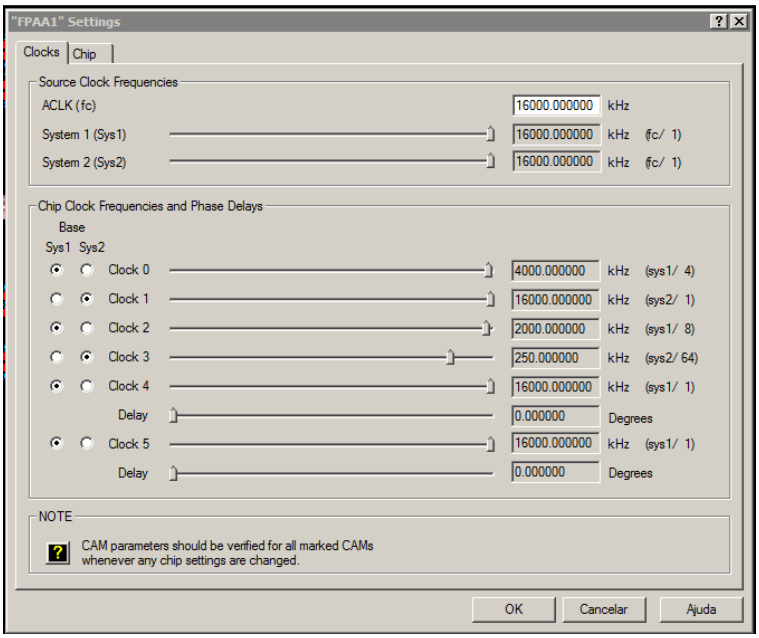


Figure 2.48 Clock base settings for dpASP AN231E04.

Having two base clocks allows for creation of two unrelated analog signal processing circuits within a single device. Clock frequency is a fundamental parameter in the function of SC analog circuitry. It should be take care that later changes in frequency parameters could affect the desired operation of the SC circuits.

2.4.5 SRAM

There are three regions of volatile SRAM within the device. The first, Shadow SRAM, is the memory that gets written to during configuration or reconfiguration. Shadow SRAM serves as a temporary holding area for configuration data prior to its transfer into Configuration SRAM. The second region, Configuration SRAM, controls the behavior of the analog signal processing circuitry. The transfer from Shadow SRAM to Configuration SRAM happens in a single clock cycle, minimizing disturbance to the analog signal paths. The third region of memory is the Look-Up Table (LUT).

2.4.6 LOOK UP TABLE (LUT)

The device contains a Look-Up Table (LUT) memory. The LUT provides replacement values for Configuration SRAM locations. A CAB plus LUT combination can be used to create non-linear functions such as arbitrary waveform synthesis and table based sensor linearization functions.

In the following example, the transfer function is a sine function converted into a triangular wave output, as shown in Figure 2.49.

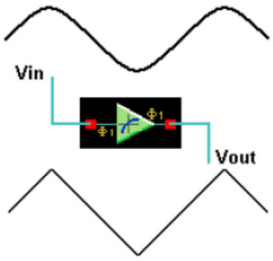


Figure 2.49 Effect sine transfer function [30].

The transfer function CAM works by digitizing the input voltage, and using the resulting digital word as the address for a LUT (LUT - 256 x 8-bit RAM). The data word from the LUT is then converted back to an analog output voltage. The analog to digital conversions are carried out by an 8 bit ADC and 8 bit DAC as shown in Figure 2.50.

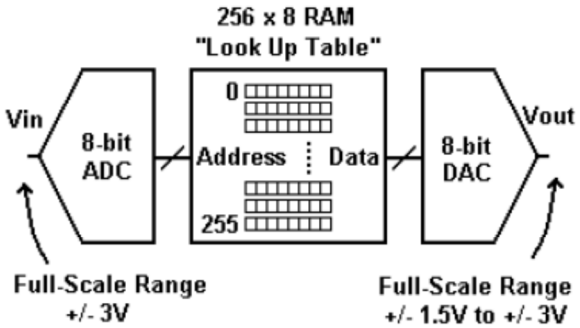


Figure 2.50 Block diagram of transfer function CAM [30].

The 8-bit ADC on the front-end has a full-scale range of +/-3 V as the input voltage is swept from -3 V to +3 V the LUT address sweeps from 0 to 255 (decimal). The content of the LUT (the data) is completely arbitrary and user defined. The data is converted to an analog output voltage with an 8-bit DAC whose full-scale range is flexible between +/-1.5 V and +/-3.0 V. The transfer function stored in the LUT consists of 256 floating-point numbers and may be input manually or loaded from a CSV file (format with numbers separated by commas) via the AnadigmDesigner 2.

2.4.7 SAR ADC

The CABs have an 8 bit successive approximation register of type analog to digital converter (SAR-ADC). The SAR-ADC requires two clocks frequencies in the ratio of 16 to 1. The lower frequency clock, Clock A determines how often successive conversions occur. The highest frequency Clock B is used to ADC input conversion.

The result of the SAR-ADC output can be directed to the port addressing of the LUT (most commonly used) or can be redirected to the CAB that generated it. At each conversion, the ADC result of 8 bits is recognized by the LUT as a new address. The circuit sets the contents of the LUT appointed this address in one or two specific positions of the transfer SRAM (Shadow SRAM).

A possible practical use of the SAR-ADC is when an input signal needs to be linearized or calibrated using LUT. As typical example, a signal from non-linear temperature sensor is connected to the SAR-ADC of a CAB, which ADC conversion result is sent to the LUT and afterwards linearization table converts to a value that is linear related with temperature measured. Synch output is logic “1” when serial conversion byte is send to data output. Figure 2.51 shows block diagram of SAR-ADC.

Figure 2.51 Block diagram of SAR-ADC CAM.

2.5 DISCUSSION

This chapter made an overview of available technologies and solutions used for FPAA construction. It is noticeable that most of academic FPAA projects are based on the continuous time principle basically using OTAs, while the currently commercially available circuits mainly from Anadigm work on discrete time SC principle. One reason for the popularity of SC technology is the fact that SC circuits allow to obtain a wide span of the parameter change by means of the switching frequency tuning. Academic projects are more concentrated in CT technology because it provides higher bandwidth, necessary for image processing and wireless applications.

It was focused attention to the AnadigmApex third generation of FPAA/dpASPs AN23x devices concerning internal block description, since the second generation AnadigmVortex was discontinued.

We can expect that the FPAA part will be gradually incorporated into the complex system on chip. We can observe this trend in subsequent generations of the Cypress Programmable System on Chip (PSoC). The mixed systems based on PSoC or a combination of the FPAA circuits with a digital system is now popular in prototype applications and it is in growing phase. In a mass production of electronic systems most of solutions is based on Application Specific Integrated Circuits (ASIC). It was described the dynamic reprogrammable and reconfigurable technology on the fly available on the dpASP from Anadigm, we can foresee that in the nearest future this dynamic reconfigurable analog cells will be parts included in ASICs.

Nowadays, the FPAA circuits are a very comfortable and flexible platform for rapid prototyping and the scope of next chapter will describe the hardware development platform from Anadigm and the programing software environment.

3 FPAA–APPLICATIONS

The use of FPAAs has increased its implementation, particularly in areas:

- Sensor and signal conditioning interface.
- Signal filtering.
- Automation and industrial control.
- Monitoring and medical diagnostics.
- Precision control.
- Ultra low frequency signal conditioning.
- Analog signal processing.
- Identification of radio frequency signals, radio frequency Identification (RFID).
- Audio signal conditioning (filtering effects, subwoofers, synthesizers, etc).

This chapter describes the main features from the third generation development board used on this Thesis and AnadigmDesigner 2 software used for device FPAA/dpASP programing and circuit simulation. Also, it is mentioned several signal conditioning methods for I/O interfacing and various sensor interface examples. Finally, it will be presented several types of applications, in order to compare the simulation results with practical results from the hardware implementations.

3.1 ANADIGMAPEX DEVELOPMENT HARDWARE

The AnadigmApex development board is an easy-to-use platform designed to implement and testing analog designs on the Anadigm FPAA/dpASP silicon devices. As the device included on this development board is a third generation dpASP AN231E04, then all explanation will be focus on this component. However, the development board could use also the FPAA AN131E04. Schematics and picture can be consulted on Appendix C.

3.1.1 MAIN FEATURES OF DEVELOPMENT BOARD AN231K04-DVLP3

The board footprint has physical dimensions 4.8 x 3.8 inches. It possesses standard USB serial interface for downloading AnadigmDesigner2 circuit files, has the ability to store configurations into onboard non-volatile memory, configurations in the onboard microcontroller Microchip PIC 16F876A with FLASH, which can be used as the boot circuit. Also has ability to write to and then boot from EEPROM (external EEPROM is not supplied, empty socket is onboard). Additional features are implemented on this board that was used on older versions from Anadigm, such has:

- Small footprint.
- Large breadboard area around the AN231E04 device.
- Header pins for all dpASP device analog I/Os.
- Ability to separate, electrically and physically, the digital section.
- Two circuit footprints for configuration as Rauch filters, single to diff converters, level shifters, etc.
- Daisy chain capability, that allows multiple boards to be connected to evaluate multi-chip systems.
- Standard PC serial interface for downloading AnadigmDesigner2 circuit files.
- On-board 16 MHz oscillator module.

3.1.2 LAYOUT OF DEVELOPMENT BOARD AN231K04-DVLP3

Figure 3.1 shows the layout of the board allowing easy location of all the components, power connections and jumpers.

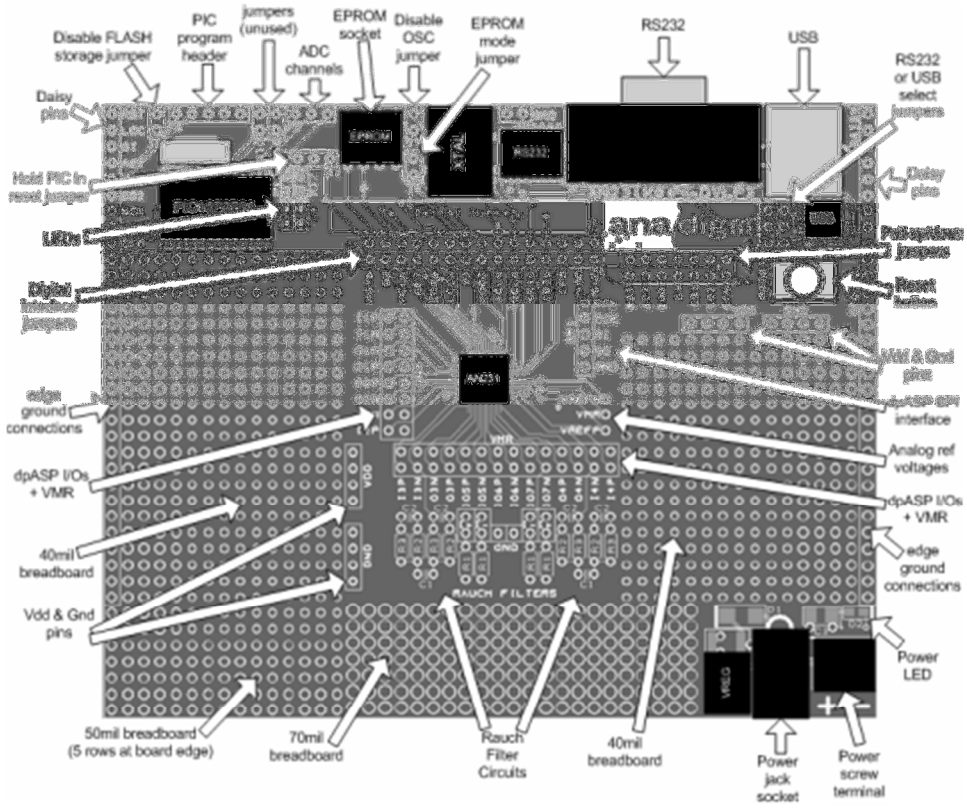


Figure 3.1 Development board AN231K04-DVLP3 [34].

3.1.3 POWER UP ANADIGMAPEX DEVELOPMENT BOARD

The board power up is implemented by connecting a transformer with voltage between +4 V and +12 V to the jack socket input or connect wires from a single precision regulated supply to the on-board 2-way terminal with the voltage set to between 4 V and 12 V.

Anadigm recommends the use of a standard supply regulator or DC power supply with a regulated output of either 6 V or 9 V DC. The board is protected against connection to a supply with the wrong polarity and should not be powered with more than 12.5 V. There is a green LED to indicate that the board is successfully powered up. It should consume approximately

25 mA when first powered up and before the dpASP (AN231E04) is configured. The current after the dpASP is configured depends very much on the circuit programmed into the dpASP.

3.1.4 INTERFACE PROGRAMING ANADIGMAPEX DEVELOPMENT BOARD

It is possible to physically connect both the RS232 and USB cables at the same time, however only one or the other is needed; should be used one of the options and set the shorting link on the Development board appropriately to enable either USB or RS232.

Anadigm prefers the RS232 because it is hardware detected and automatically discovered by AnadigmDesigner2 software, however as many new PCs do not have RS232 interface, then the USB interface is used additionally with installation of all the associated drivers.

3.1.5 MULTI-CHIP DESIGNS – DAISY CHAINING

In most of the designs, it is required more than one FPAA/dpASP to realize more complex circuits. Figure 3.2 shows an implementation of two boards connected together as daisy chain configuration. More boards can be chained using the instructions on the same figure.

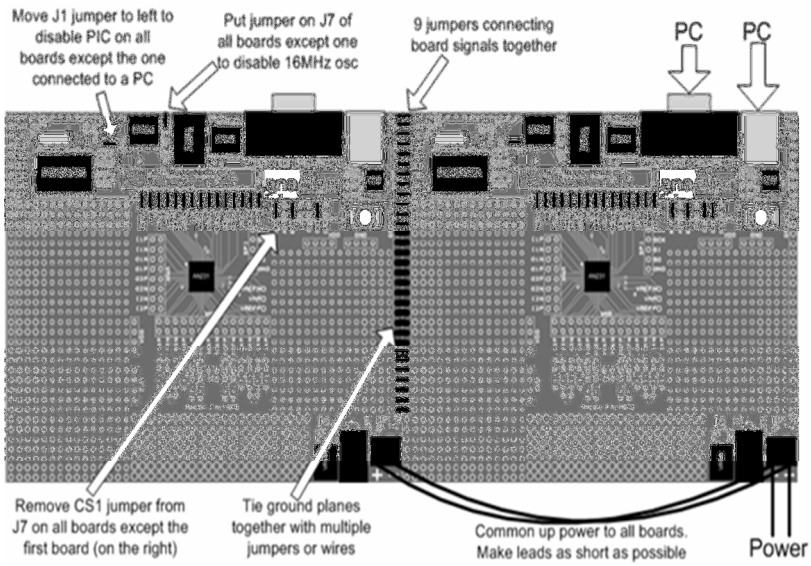


Figure 3.2 Daisy chain configuration with two development board [34].

3.1.6 ADDITIONAL IMPORTANT FEATURES

Three reference pins on the dpASP device – VMR (+1.5 V), VREFP (+2.5 V) and VREFN (+0.5 V) have been connected via the PCB tracks to the 3 holes to the right of the dpASP (see Figure 3.2). In addition, VMR is available on the inner ring or inner two rows of pins that are adjacent to the analog I/Os. These reference voltages are not designed to provide current.

HEADER PINS

All analog I/Os of dpASP are brought out to header pins for easy connection. Next to these header pins is a second row of header pins connected to VMR (+1.5 V). This allows the user to connect any dpASP analog I/O to VMR using shorting jumpers, resistor jumpers or capacitor jumpers. A shorting link (jumper) should only be used when the I/O cell is configured as an input. Damage may occur to the device if an output if shorted to VMR.

EEPROM

There is an SPI EEPROM socket in the digital section of the board since EEPROM integrated circuit it is not supplied with Development Kit. To use an SPI EEPROM it should be placed into the socket on the board and programmed with configuration file. An example of a compatible SPI EPROM is the Atmel AT25080.

RESET BUTTON

There is a reset button near the upper right corner of the board. This resets both the dpASP and the PIC (unless the PORb jumper is removed from J5 or the J1 jumper is in the left position). In EPROM mode, it should be pressed the reset button to load the circuit from the EPROM into the dpASP.

SPI PORT

There is an SPI port for direct control of dpASP by an external SPI controller. All jumpers should be removed from J5 when the SPI port is used.

3.2 ANADIGMDESIGNER 2 DEVELOPMENT SOFTWARE

Anadigm second-generation development environment, AnadigmDesigner 2 EDA tool provides the possibility to design and implement dynamically reconfigurable analog circuits in short development time. The circuit is implemented by dragging and dropping Configurable Analog Modules (CAMs), each of which can be used to implement a range of analog functions. AnadigmDesigner 2 includes a time domain functional simulator which provides a convenient way to assess the circuit behavior without need of hardware set-up. The simulator user interface is intuitive. It is possible to build a complete analog system rapidly, simulate it immediately and then just point and click to download it to an FPAA chip for testing and validation.

3.2.1 USER INTERFACE

AnadigmDesigner 2 presents the user with an intuitive interface with few icons push-button shortcuts provided in a palette. Design window contains a view of the FPAA devices showing the external pins (numbered for easy reference), their associated Input and Output cells, and a large central region which can be populated with CAMs and wiring. Figure 3.3 shows the environment development.

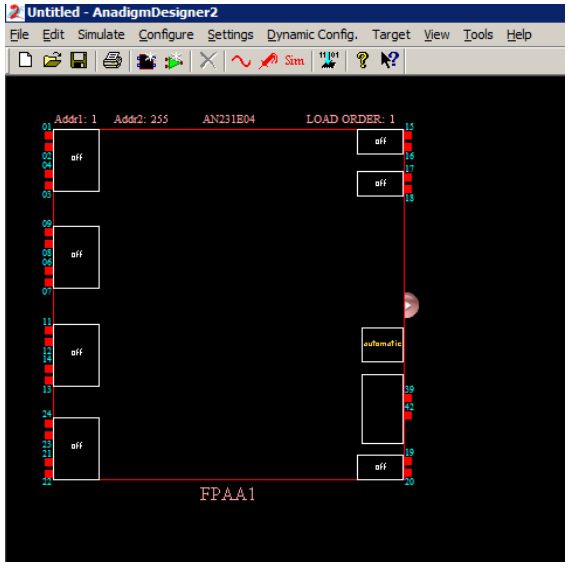


Figure 3.3 New design for device AN231E04.

When first time invoked, the program displays a docked pallet of tool buttons associated with the most commonly used functions of the software just below the pull-down menu bar. Figure 3.4 shows the pallet with correspondent description of function and shortcut button information, undocked from design window.

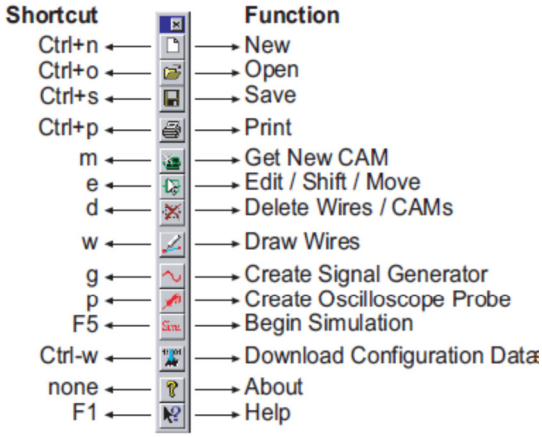


Figure 3.4 Pallet icons with shortcut buttons.

All of the menu items associated with each of the pull-down menus and contents available within AnadigmDesigner 2 are shown on Figure 3.5.

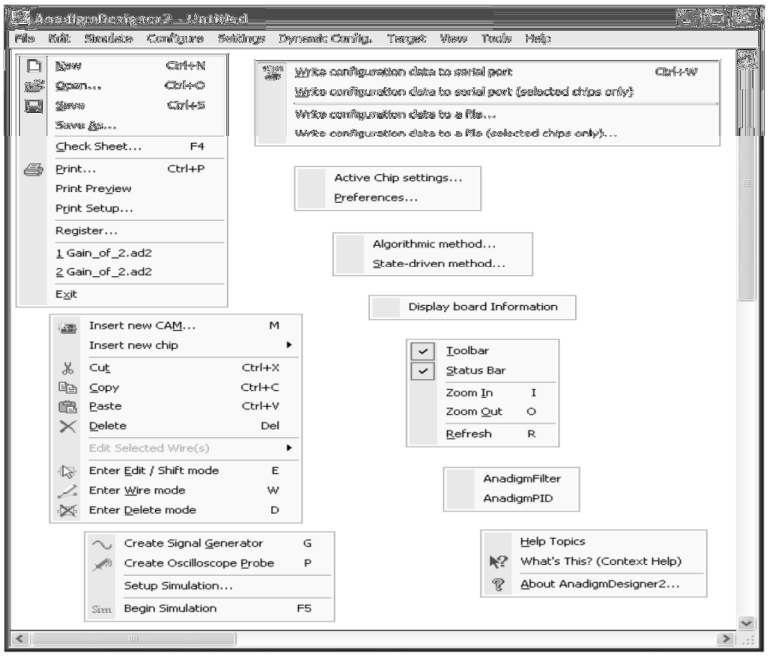


Figure 3.5 An overview of all available menu items.

3.2.2 PROJECT IMPLEMENTATION

We now proceed to explain the functionality of AnadigmDesigner 2 environment, version 2.8.0.1, released in August, 2014. It is created a new project for implementation of a single bilinear filter stage. The next steps should be followed:

1 Open AnadigmDesigner 2 Software.

2 Should be selected "**settings**" menu and select "**preference**".

3 Select the default chip type as AN231E04 and set the master clock as 16 MHz, as shown in Figure 3.6.

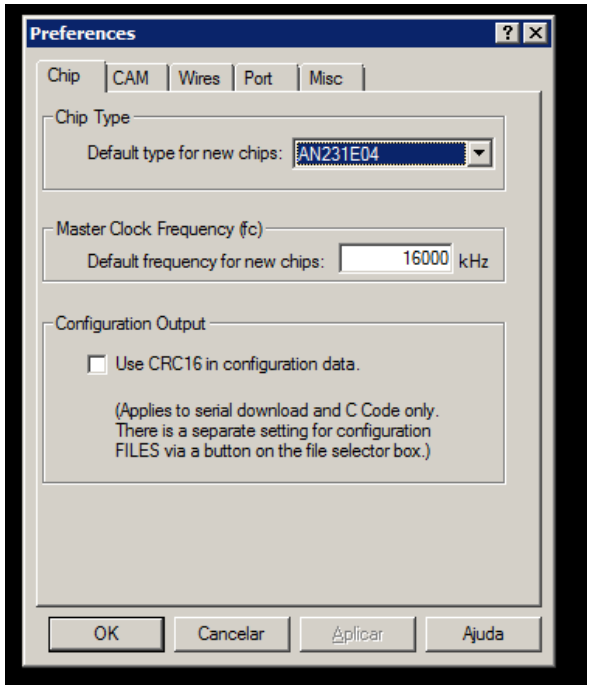


Figure 3.6 Chip settings.

4 Select the "**Port**" tab; select port as "**COM3-CP2101 USB to UART bridge controller**" form the drop down list. Click "**Apply**" button, as shown on Figure 3.7.

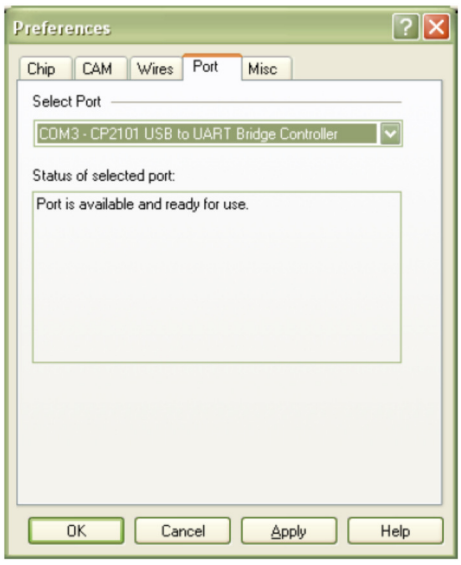


Figure 3.7 Port settings.

The driver for "CP2101 USB to UART bridge controller" should be installed in the computer to establish communication with FPAA board. Also, it is necessary to connect the powered board to computer to get the COM3 option enabled in the drop down list.

5 "**File**" menu and select "**New**".

6 For selecting Configurable Analog Modules (CAMs), "**Edit**" menu and select "**Insert new CAM**", as shown in Figure 3.8.

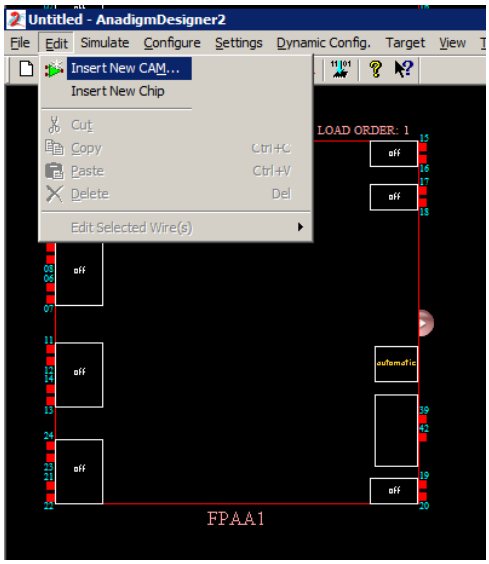


Figure 3.8 New CAM insertion.

7 Then CAM browser will be visible. From the CAM browser, it is selected filter bilinear, as shown in Figure 3.9.

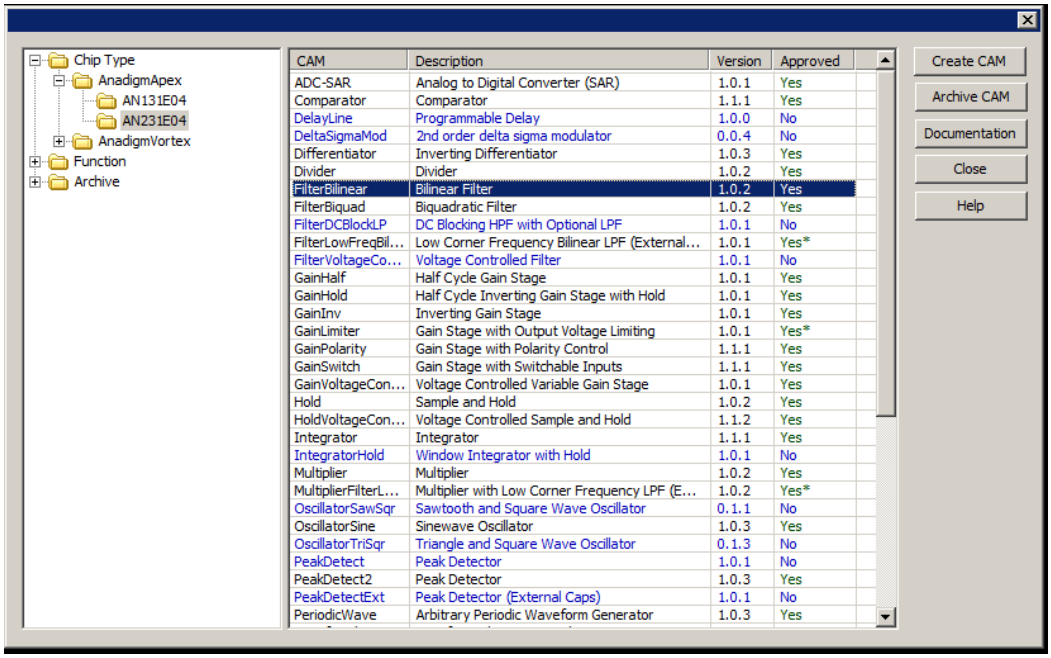


Figure 3.9 CAM selection.

8 The CAM should be placed inside FPAA design, then parameter setting window becomes visible. Clock A is selected to 4000 kHz and gain set to 1, and corner frequency to 400 kHz, as shows Figure 3.10.

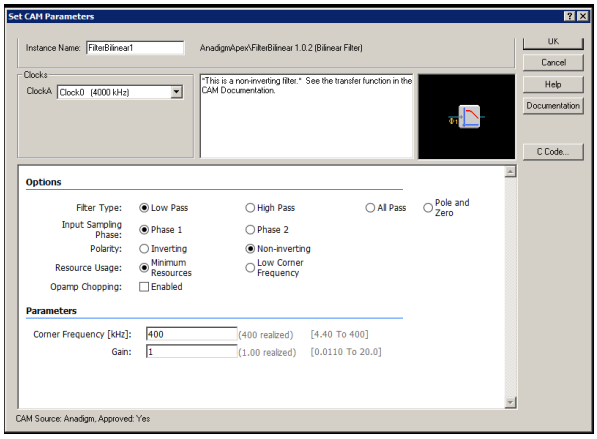


Figure 3.10 Setting CAM parameters.

If some setting parameter is out of range then appears in red color. For instance, if the corner frequency is higher than 400 kHz then the box appears in red color and parameter should be reduced to a value inside the range.

9 CAM is connected to I/O ports through wires (Figure 3.11).

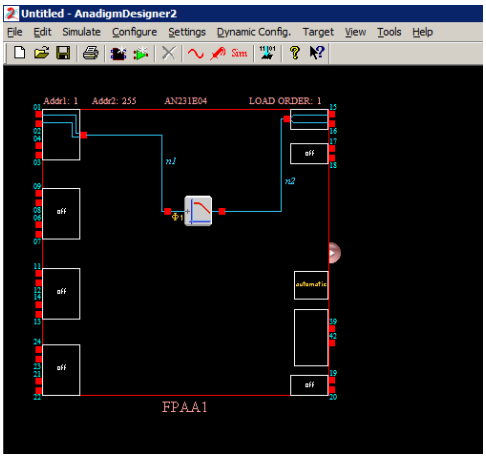


Figure 3.11 Connecting CAM to the ports.

A double click on the I/O cells, which opens a window where the ports are configured as input or output.

10 For simulation purposes, input signal can be applied to the I/O Cell 1. For creating a signal generator, on simulate menu is selected “Create Signal Generator” and then is attached the signal generator with input cell.

11 For setting the parameters of the input signal double click on the signal generator. The setting window is shown in Figure 3.12. The frequency oscillator is set to 200 kHz.

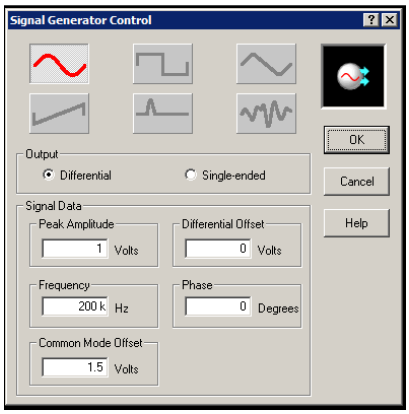


Figure 3.12 Setting window for signal generator.

FPAAs input voltage range is 0 V to 3 V, then amplitude input signals are less than 1.5 V. The Common Mode offset of 1.5 V should be set to make the range within 0 V to 3 V. Input and output ports are differential, so it should be taken care to give differential input signals from the signal generator. Output ports are differential, so it will give differential output signals only.

With the development board, an extra circuitry is built to convert the given single ended input signal to differential ended signal to connect to the input FPAA. Also, the additional signal conditioning extra circuit will convert the differential output signals from the FPAA to single ended signals.

12 To connect the oscillator probes is selected "**simulate**" menu and then selected "**create oscilloscope**" and then should be connected to wherever necessary.

13 For simulation, the oscilloscope probes are connected to the input and output of the CAM (Figure 3.13).

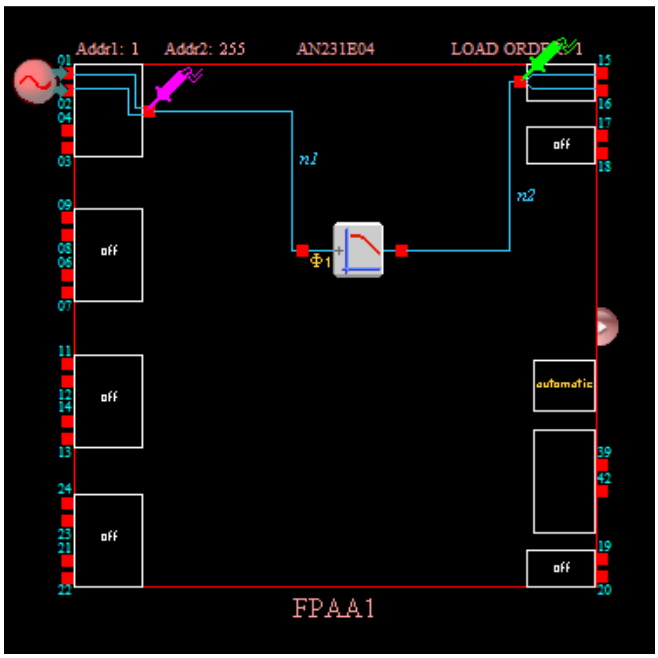


Figure 3.13 Connecting oscilloscope probes.

14 Simulation is done by "**simulate**" menu and select "**Begin Simulation**".

15 The simulation window of AnadigmDesigner2 software is shown in Figure 3.14 and Figure 3.15 for two distinct input frequencies. The response to input frequency 200 kHz is shown in Figure 3.14. Practically, no signal attenuation is seen.

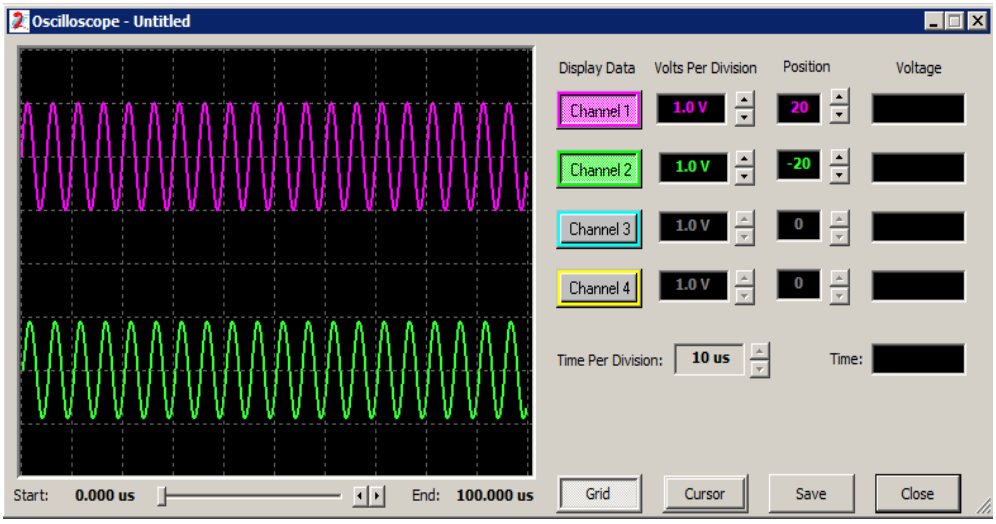


Figure 3.14 Response of bilinear filter to input frequency 200 kHz.

The response to input frequency 600 kHz is shown in Figure 3.15. It is seen an attenuation on the amplitude of output signal, because the input frequency is higher than the corner frequency of bilinear low pass filter.

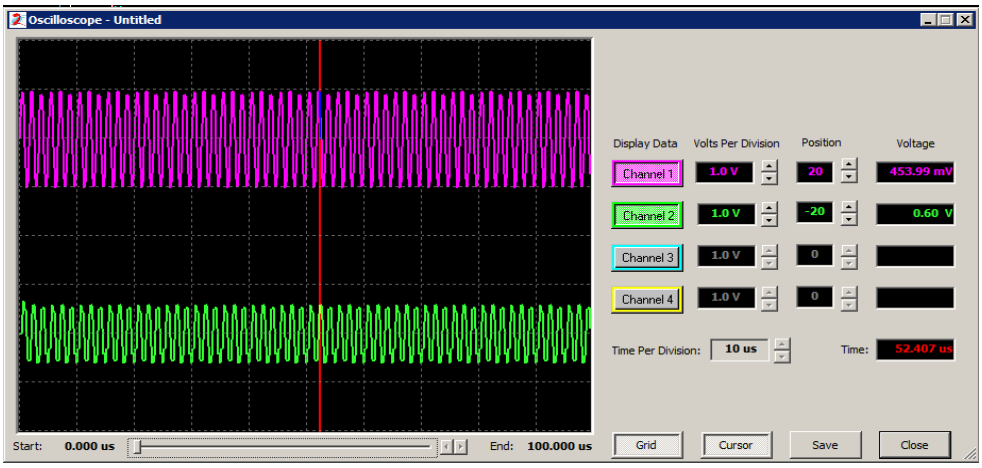


Figure 3.15 Response of bilinear filter to input frequency 600 kHz.

If we move the cursor to the peak value of the output signal wave, the voltage value is 0.6 V. The input signal was set previously to 1 V peak.

16 Once satisfied with the simulation result, the design circuit could be downloaded by two means. One way is to download the configuration bit stream through USB port provided along with the board. For that, select the download button on the window panel or select "**Configure**" menu and then "**Write Configuration data to serial port**" as shows Figure 3.16.

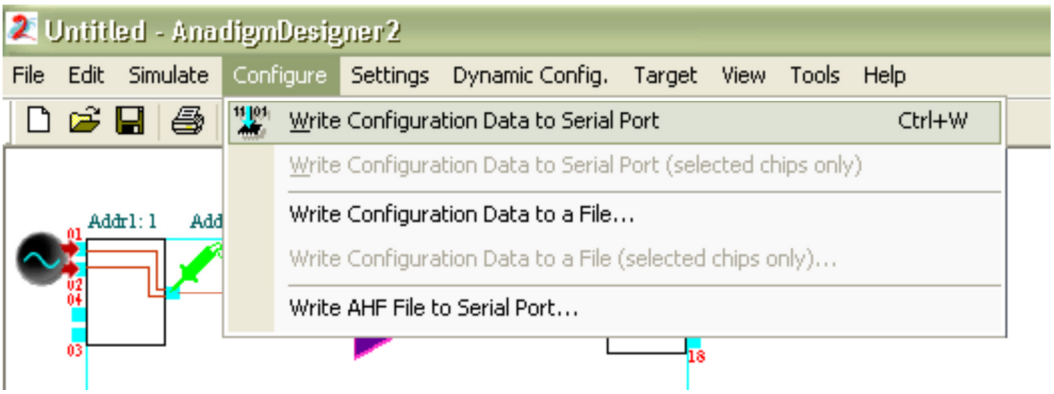


Figure 3.16 Programming FPAA through USB.

17 The second way is to save configuration bits of the design. It is mainly used for downloading the design into EEPROM, if installed on development board. Select "**configure**" menu and chose "**Write Configuration data to file**", as shows Figure 3.17.

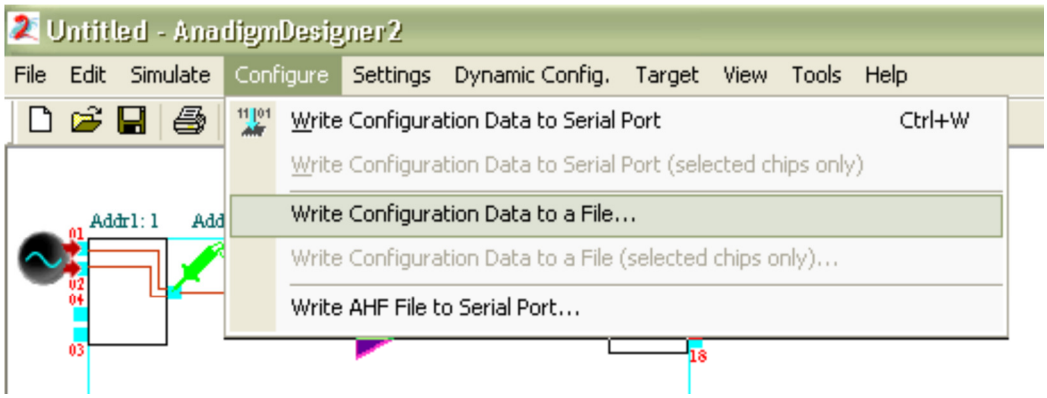


Figure 3.17 Writing configuration data to a file.

From the pop up window should be selected the "Binary File [*.bin]" as save type to save the configuration data. Then the saved file can be downloaded into EEPROM using a programmer tool. This method will not be used as the download method, it will be done by USB. Anyway, the development board has an empty socket (8 pin), to install a programmed EEPROM with this saved [*.bin] file.

3.2.3 CONFIGURABLE ANALOG MODULES (CAMS)

Configurable Analog Modules or CAMs are circuit building blocks abstracted to a functional level that can be manipulated in AnadigmDesigner 2. Complex circuits can be implemented in a chip simply by selecting, configuring, placing, and wiring CAMs. They contain multiple circuit parameters and architectures that can be selected though CAM configuration. However, the user is not required to understand the underlying fundamental circuits that are incorporated into the CAMs because they have been abstracted to a functional level at the user interface. This improves the speed and ease of circuit design.

Every CAM is a member of a CAM Library. The left side of the select CAM window lists all of the libraries that are available in the system. By selecting the name of family, function, archive, or particular chip library, all of the relevant CAMs will be listed on the right.

The CAM Browser has intelligence that allows it to know which CAMs will work in which chips thus simplifying the CAM selection process. The CAM browser will display the CAM file name, the descriptive name of the CAM, the CAM version number, and the approval status of the CAM. An asterisk in the "Approved" field means that the CAM is approved but contains non-standard features. Figure 3.18 shows the CAM browser.

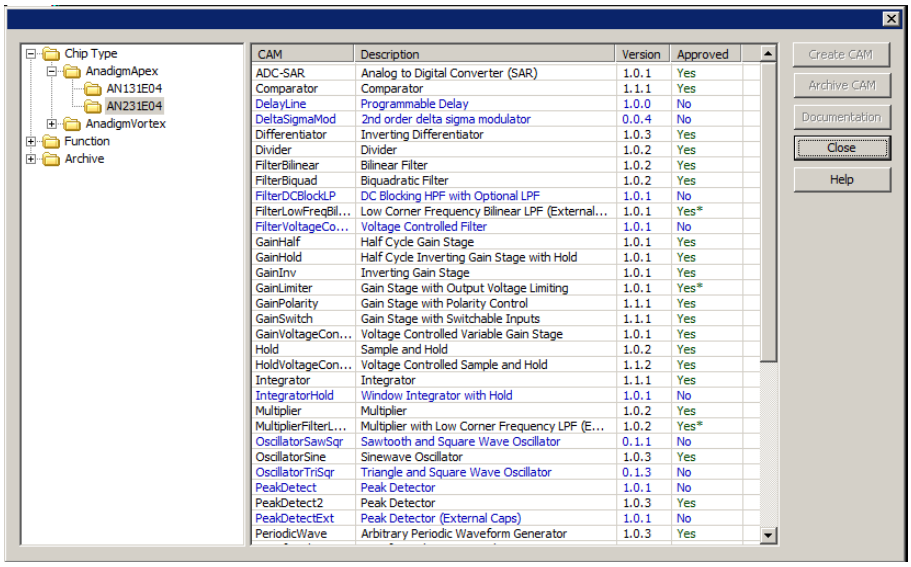


Figure 3.18 CAM browser selection.

To create CAMs and add them to design, select and click the "**Create CAM**" button. This will create a new instance of the selected CAM and allows placing it on circuit. It is also possible to drag CAMs from the CAM selection window directly onto design. This allows creation of many CAMs without having to close the CAM selection window. Figure 3.19 shows two example circuits with correspondent CAMs interconnected by wiring. Each CAM has its function description on top of the symbol.

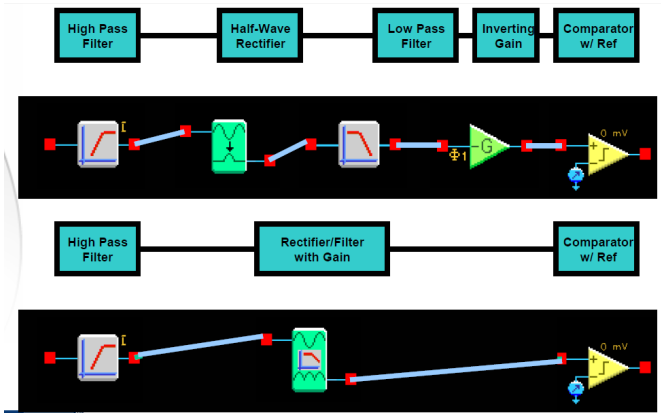


Figure 3.19 Example of circuit design with CAMs [35].

Complex circuits can be implemented by selecting, configuring and wiring CAMs. Each CAM has a user interface to set options and limits. Each CAM has an accurate model for use in time-based simulator. Custom CAMs can also be built for specific applications.

3.2.4 FUNCTIONAL SIMULATOR

AnadigmDesigner 2 functional simulator is included to facilitate circuit design and experimentation without the need for any lab equipment. The simulator features an intuitive user interface and displays time domain results graphically. The steps to develop and test the circuits are:

- Wire up circuit.
- Attach and set up signal generators.
- Attach oscilloscope probes.
- Set up the simulation parameters.
- Launch the simulator.
- Check results to verify if they are according expected.

CAM simulation equations are contained as text strings within each CAMs. For CAMs included with a particular software release, the simulation equations also reside in a compiled form within the executable files of the system. The compiled equations are used whenever available and greatly increase the speed of the simulator. If a compiled simulation model is not available (a user defined CAM, or a CAM created after a software release) then the simulator will evaluate the simulation equations within the .cam file using a run time interpreter and then simulation speed will be noticeably slower.

To setup simulation, the pull down menu "**Simulate**" and "**Setup Simulation**" allows establishing the start and stop time of simulation run. Figure 3.20 shows the setup window for the simulator.

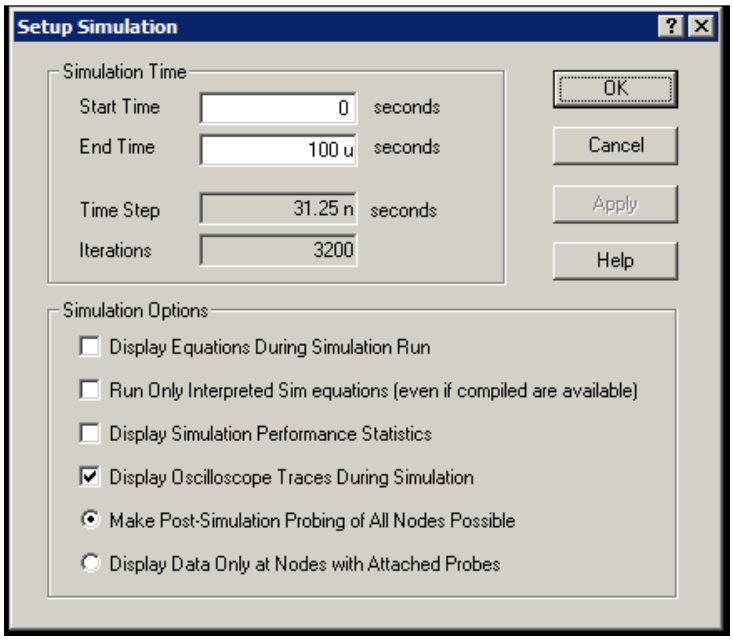


Figure 3.20 Setup window for simulator.

The "**Time step**" parameter is automatically calculated and inserted for you as 1/2 the period of the fastest System Clock frequency (fsys). "**Iterations**" refer to the number of simulation steps. Time step and number of iterations is only adjusted after selecting "**OK**". Launching the simulation is accomplished using the pull down menu selection "**Simulate**" and then "**Begin**". "**Display Equations during Simulation Run**" is similar to single stepping through the simulation. This feature is typically only invoked by advanced developers. The simulation performance statistics can be used to show how long the simulation is taking, how often each particular CAM is running, and whether any of CAMs are running interpreted simulation code. All node data can be saved for post simulation exploration.

All the simulation results are now available for graphical analysis. Each of the waveforms is color keyed to each of the scope probes dropped in the circuit. The display of each waveform can be toggled on and off by pressing its associated "Channel" button. The signal amplitude display scale can be adjusting using the associated "**Volts Per Division**" control. A "Position" control is also available that allows to separate the waveforms vertically for easier viewing. Figure 3.21 shows the simulation oscilloscope display with the wave shape results.

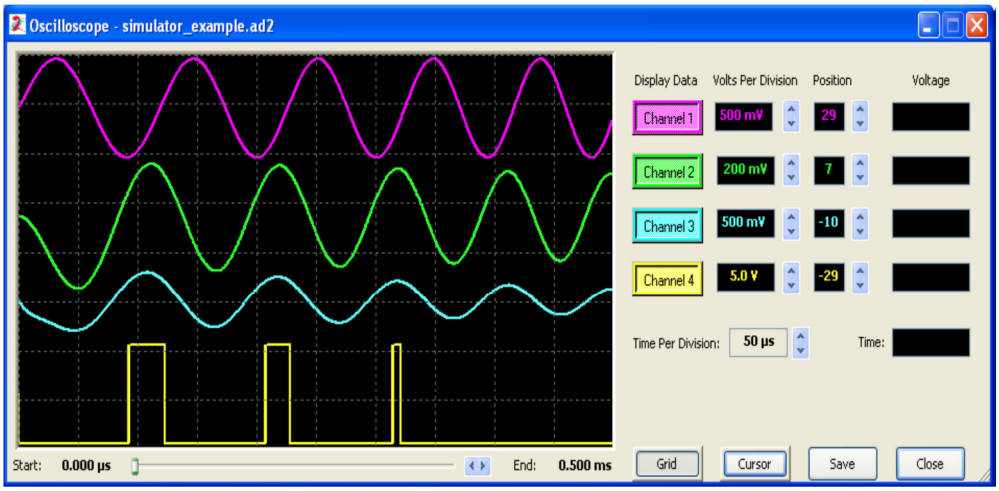


Figure 3.21 Oscilloscope display showing a simulation example.

A single vertical cursor is available to drag left and right within the waveform window. There are four "**Voltage**" displays, one for each waveform and a single "**Time**" indicator. As the cursor is moved horizontally, the voltage and time indicators all update to reflect that instant simulation results. Moving the waveforms up and down using the "Position" control does not affect the voltage readings.

3.2.5 ANADGIM TOOLS (ANADIGMFILTER AND ANADGIMPID)

Besides the main development interface, Anadigm offers two additional tools to the user. The first one is AnadimFilter that creates filters of several types and orders. Second is AnadigmPID, this tool makes available the implementation of controllers in closed-loop like Proportional Integrated Differential (PID) controllers. These tools have an advantage to send automatically the configuration to AnadigmDesigner 2 design or hardware platform.

ANADIGMFILTER

AnadigmFilter permits to help the filter design. The filters available for section are:

- Butterwoth.
- Chebyshev.
- Inverse Chebyshev.
- Elliptic.
- Bessel.

Regarding bandwidth filtering type, it is possible to select:

- Low Pass.
- High Pass.
- Band Pass.
- Band Stop.
- Custom.

The best way to explain the tool is to use an example. Considering the filter project information:

- Butterworth low pass filter.
- Band Pass Ripple of 3 dB.
- Pass Band Gain of 0 dB.
- Stop Band Attenuation of 63 dB.
- Pass Band Frequency, 1 kHz.
- Stop Band Frequency, 4 kHz.

These data configuration is represented in Figure 3.22, where it is possible to observe the frequency response and Pole and Zero Plot complex location in tool designer.

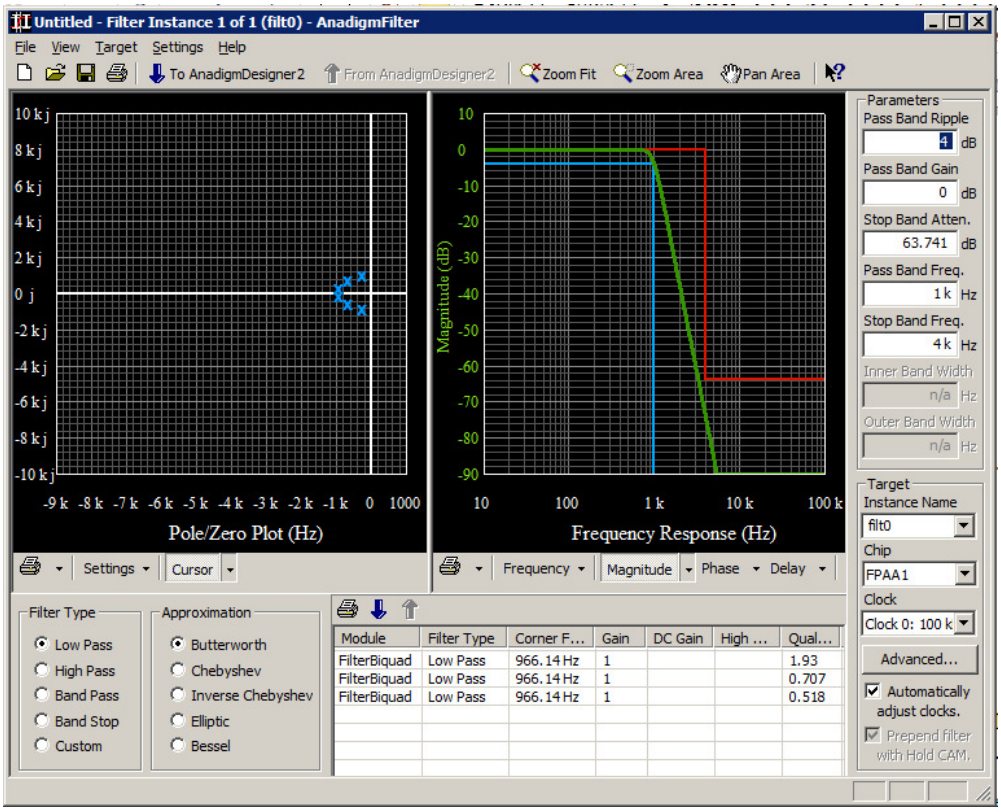


Figure 3.22 AnadigmFilter design of Butherworth filter.

After getting the required settings and design response, it is possible to export to AnadigmDesigner 2, as shown in Figure 3.23.

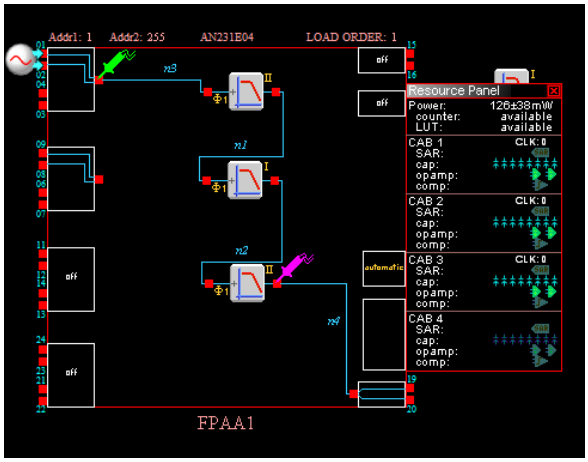


Figure 3.23 Butherworth filter exported to AnadigmDesigner.

After getting the design exported, it is possible to simulate the behavior of the circuit by simulation for an input generator setting of 200 kHz sinusoidal signal, as shown in Figure 3.24.

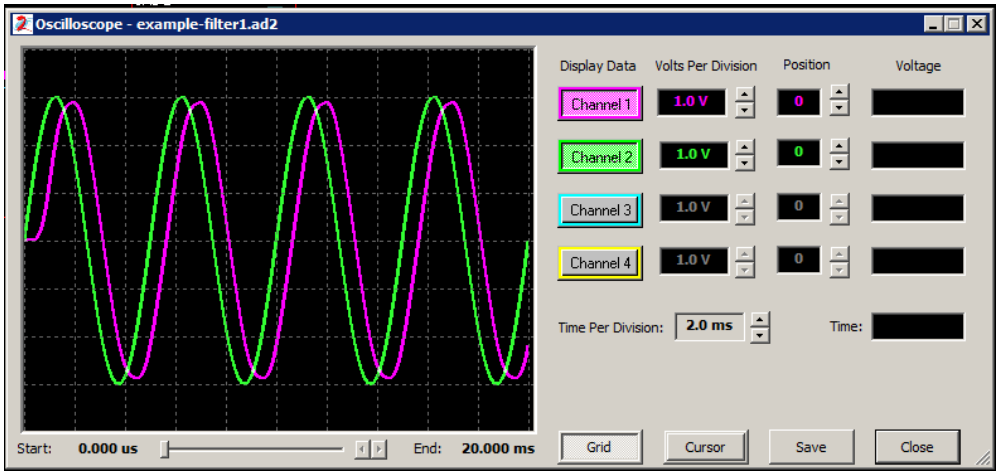


Figure 3.24 Butherworth filter simulation result.

The result wave in pink color shows an initial delay and phase delay. The input signal has 3 V amplitude. The simulator also shows that output signal has a small attenuation.

ANADIGMPID

Unfortunately for the third generation device, this tool shows that is not available. Figure 3.25 shows the message " No compatible chips found".

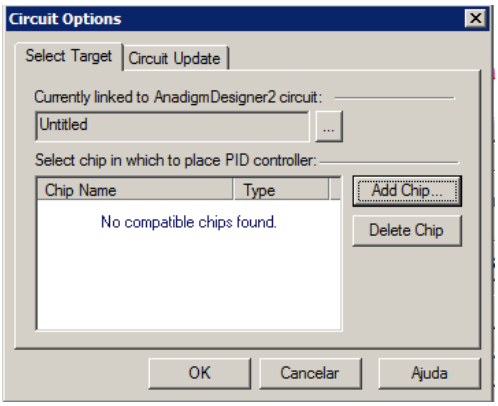


Figure 3.25 Message of AnadigmPID when is selected AN23X device.

Anyway, the possibilities of this tool for AN22X second generation are very flexible, as demonstrated in Figure 3.26.

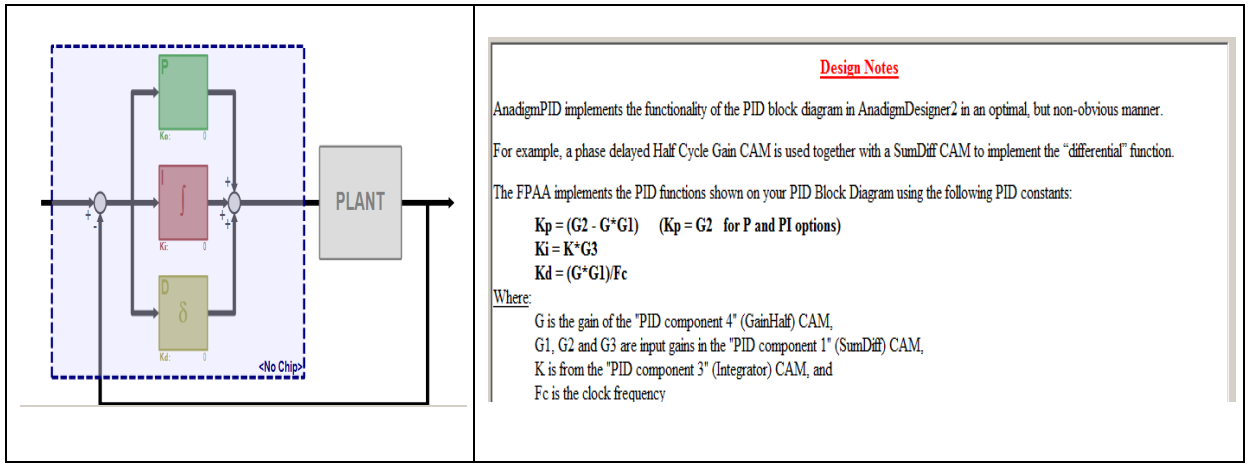


Figure 3.26 AnadigmPID designer.

It should be considered that transfer function of PID controller is mentioned on the tool as expressed in Figure 3.27, where K_0 is proportional gain, K_i is the integral gain and K_d the differential gain.

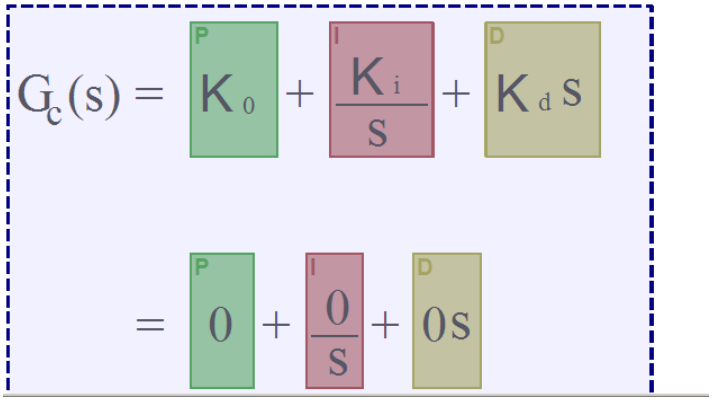


Figure 3.27 PID transfer function.

3.3 ANALOG SIGNAL CONDITIONING FOR I/O ANADIGM FPAA/DPASP

Due to the fact that, there are different kinds of sensors with variety of their output signals and different types of actuators with special needs of input signals, it is necessary to develop special hardware to perform the signal conditioning between the external devices and the input/output pins from the dpASP.

All dpASPs are single supply devices, they work from a positive voltage supply (Vdd) and ground. There is no negative supply which means that the dpASP cannot handle signals that are negative, either on its inputs or outputs. The dpASP can only handle signals that are between ground and its positive supply. For Apex family that supply is +3.3 V. For this reason, AnadigmApex family FPAA/dpASP has an internal signal ground that is fixed at a positive voltage just below half the supply voltage. This signal ground is the Voltage Main Reference (VMR) and is set to +1.5 V. All the analog signals paths within and at the I/O of the dpASP are differential, they consist of two equal and opposite signals, both centered on VMR, and both restricted to the range of ground and Vdd.

Before describing different methods of interfacing analog signals to the FPAA, it is important to realize that the device can be used in single-ended or differential mode.

3.3.1 I/O ANALOG INTERFACE METHODS

DC biased input

If the input signal to the FPAA is single-ended and has a small unwanted DC bias but remains within the range 0 to +3.3 V, then it is possible to effectively remove this bias by applying an appropriate DC bias to the negative input of the differential pair. Figure 3.28 shows an example of a +2.5 V referenced, single-ended signal connected to the positive input and a +2.5 V DC bias connected to the negative input.

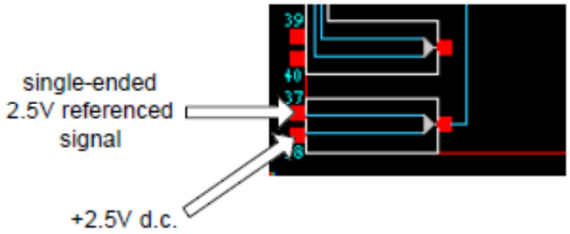


Figure 3.28 DC biased input [31].

This method has the advantage of being very simple. Its disadvantages are that it only works with single-ended signals, and only works for the input of the FPAA, the output cannot be level-shifted in a similar manner. Additionally, the input signal with its DC bias must be within the 0 to +3.3 V range.

OPAMP circuits

This method uses OPAMP circuits. Figure 3.29 shows how a ground referenced signal can be level-shifted to +1.5 V for input to the FPAA/dpASP. This circuit can also be used to attenuate large signals or amplify small signals. The gain of the circuit is given by:

$$Gain = \frac{Rf}{Ri} \tag{3.1}$$

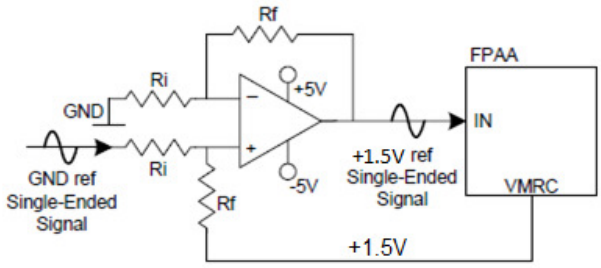


Figure 3.29 Level-shift on input [31].

The VMRC pin must not be too heavily loaded. It is recommended to keep the sum of Rf and Ri to approximately 100 kΩ. Figure 3.30 shows a single OPAMP used to level-shift the FPAA/dpASP output but also doing a differential to single-ended conversion. Furthermore, this circuit can drive devices with low input impedance and can be used to amplify the FPAA output by any desired amount. The gain of this circuit is given by equation (3.1).

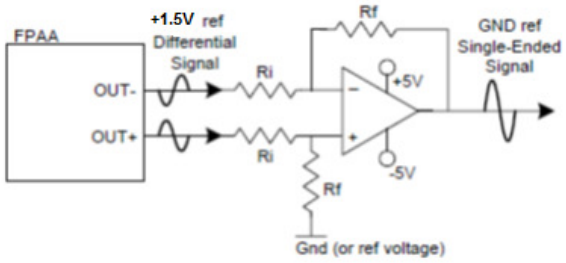


Figure 3.30 Level-shift and convert differential to single-ended signal on output [31].

The scheme shows a level shifting of the FPAA/dpASP output to ground, the resistor Rf connected to ground provides the reference for the level-shifted signal. However, this circuit can be used to level-shift the FPAA output to any desired voltage simply by connecting the resistor Rf to that voltage instead of ground.

The advantages of this method are that DC information is not lost, signals of any amplitude or DC bias can be handled and the output can drive devices with low input impedance. Also the FPAA/dpASP output can be both level-shifted and converted from differential to single-ended. The disadvantages are its dependence on resistor tolerances.

Differential OPAMPs

This method uses differential OPAMPs with common mode/reference voltage inputs. The AD8132 is an OPAMP with differential IN and differential OUT pins and a common mode input. This device can be used to level-shift and/or perform single-ended to differential conversion. Figure 3.31 shows the basic circuit for a gain of 1. The input to this circuit can be differential or single-ended, where the lower input is connected to ground.

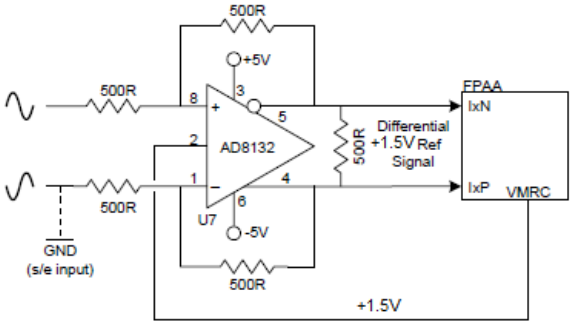


Figure 3.31 Single-ended to differential converter input to FPAA [31].

The AD8132 has very high bandwidth (350 MHz) which may cause problems due to aliasing of high frequency noise. This can be avoided by connecting capacitors in parallel with the feedback resistors. For example, 1 nF capacitors will give a corner frequency of approximately 300 kHz.

The resistor values in Figure 3.31 can be modified to change the gain of the circuit. This means that large amplitude signals can be attenuated before being input to the FPAA/dpASP. The gain equals the ratio of feedback resistor to input resistor. If a gain of 0.1 is required then the input resistors should be changed to 5 kΩ.

Figure 3.32 shows a differential to single-ended converter and level-shifter circuit. It uses the AD8130 which is a differential IN single-ended OUT OPAMP with a reference voltage input. The gain of this circuit can be modified by adjusting the values of the resistors. The gain is given by:

$$Gain = 1 + \frac{Rf}{Rg} \tag{3.2}$$

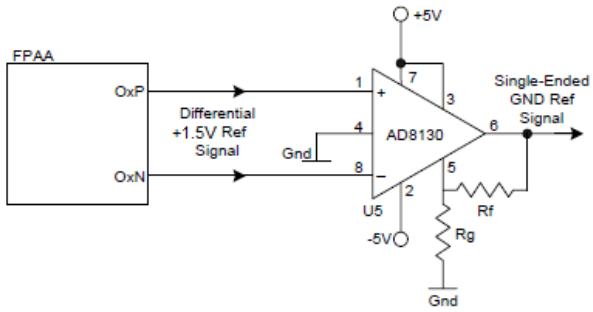


Figure 3.32 Differential to single-ended-converter [31].

For a unity gain, pin 5 should be connected directly to pin 6, this means no resistors required. The signal can be level-shifted to any voltage by connecting that voltage to the reference input pin 4 of device AD8130. This method of using differential amplifiers has the advantage of handle signals referenced to any voltage, signals of any amplitude, and differential or single-ended signals.

Chopper Amplifier

This method is used only with input differential signals which have a floating reference and small amplitude. These particular classes of signals are quite common, such as in microphones and thermocouples. The signal source should be connected directly to the FPAA input and set in 'low offset chopper' mode. The chopper amplifier amplifies the input signal by a factor in the range 16 to 128 in steps of 16, without adding any unwanted offsets to the signal. Since the chopper amplifier does not pull its inputs to +1.5 V, a pair of resistors between the differential inputs and the VMRC pin is needed as shown in Figure 3.33.

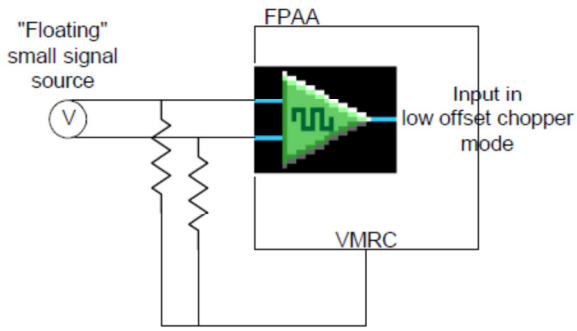


Figure 3.33 Chopper amplifier [31].

This method has the advantage of being cheap and simple with no dependence on component tolerances. Its disadvantage is that it can only be used with low amplitude floating signals.

Signal Input Using the Rauch Filter

The Apex dpASP provides an optional input OPAMP, available within I/Os 1-4 (this is not provided on second generation, Vortex family).

This I/O OPAMP allows constructing a circuit using only passive components, that performs 4 tasks:

- Level shifts an input signal bias voltage to VMR.
- Convert a single-ended signal to differential signal (if required).
- Performs a 2-pole (2nd order) low-pass anti-aliasing filter function on the input signal in order to reduce noise.

- It can amplify or attenuate an input signal in order to best match it to the input range of the dpASP.

This circuit used is called a Rauch filter (or low-pass multiple feedback filter), and is shown in Figure 3.34.

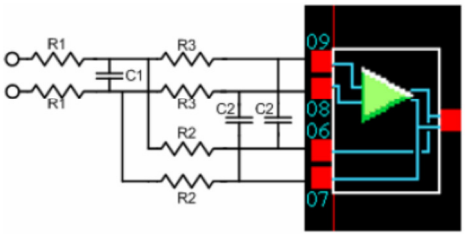


Figure 3.34 Rauch input filter [31].

The values of the components can be calculated from the required values of F_0, that is, the low-pass corner frequency, Q value of filter normally is 0.707 for optimum flat response in pass-band, and G is the pass-band gain. It should be fixed a convenient value for R1 and the equations to calculate the components are shown below:

$$R2 = R1 \times G$$

$$R3 = R1 \times \frac{G}{G+1}$$

$$C1 = Q \times \frac{(G+1)}{(G \times F_0 \times R1 \times 2 \times \pi)} \tag{3.3}$$

$$C2 = \frac{1}{(G \times F_0 \times R1 \times Q \times 4 \times \pi)}$$

The signal applied to the Rauch filter can be single-ended or differential and centered on any voltage. It can also be any amplitude and the gain Q is set to provide the correct amplitude

at the dpASP pins. The corner frequency F_0 should be set to a value just above the working range of the input signal. If a ground referenced single-ended signal is input to the Rauch, then the other input should be tied to ground.

3.3.2 SENSOR SIGNAL CONDITIONING AND PROCESSING

FPAAs are very flexible for signal conditioning provided by sensors. Figure 3.35 shows a generic block diagram regarding the available features for sensor processing signals applied for control systems.

The main design challenges for signal processing for sensors are the following:

- Sourcing stable references and stimulus.
- Multiple sensors with differing signal conditioning needs.
- Methods of calibration and maintenance.
- Manufacturing considerations.

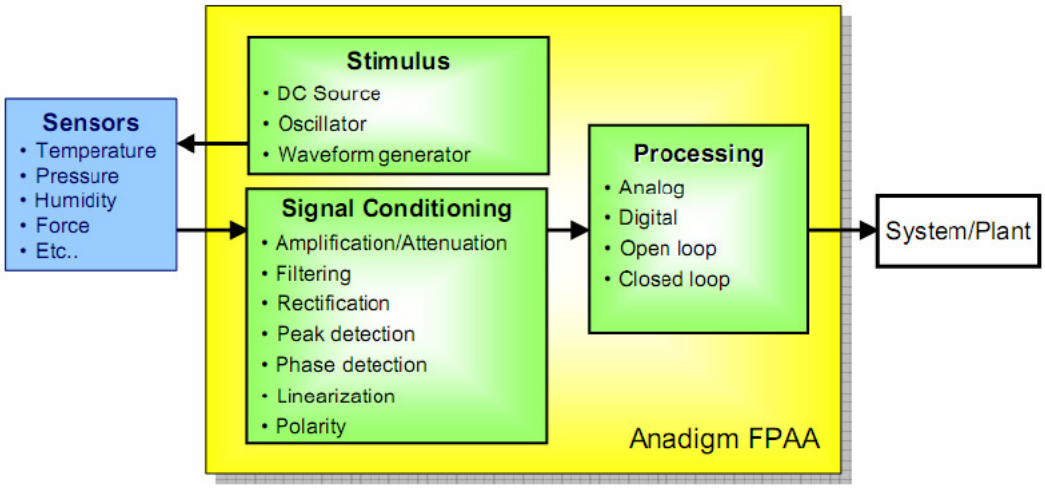


Figure 3.35 Block diagram with available features of FPAA for sensor signal processing [31].

According the previous figure, the tasks involved are amplification/attenuation, offset removal, rectification, filtering, linearization, etc. Next topics will describe several sensor types applied to FPAA and some signal processing considerations.

THERMISTOR

This sensor type has resistance range from 100 Ω to 1 MΩ and typical current less than 100 µA to avoid self-heating. Figure 3.36 shows an example for processing the signal provided by a thermistor.

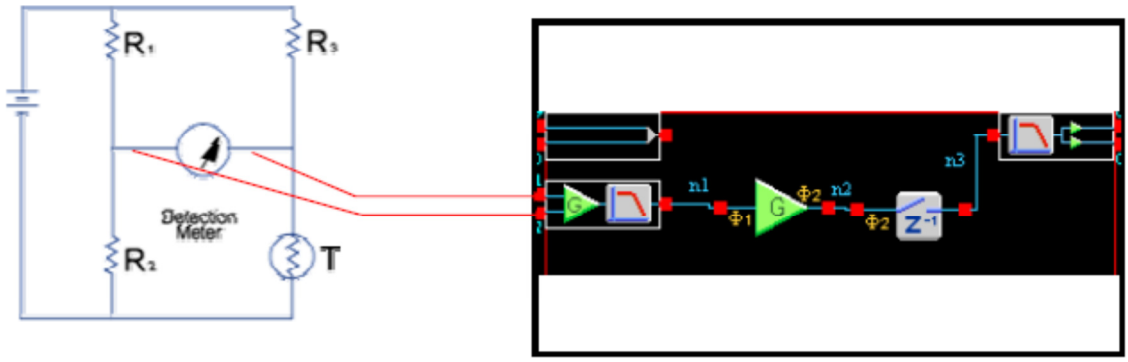


Figure 3.36 Thermistor connected to FPAA for sensor signal processing [32].

THERMOCOUPLE

This sensor type has small relation of voltage output versus temperature and high levels of common noise. Figure 3.37 shows an example for processing the signal provided by a thermocouple.

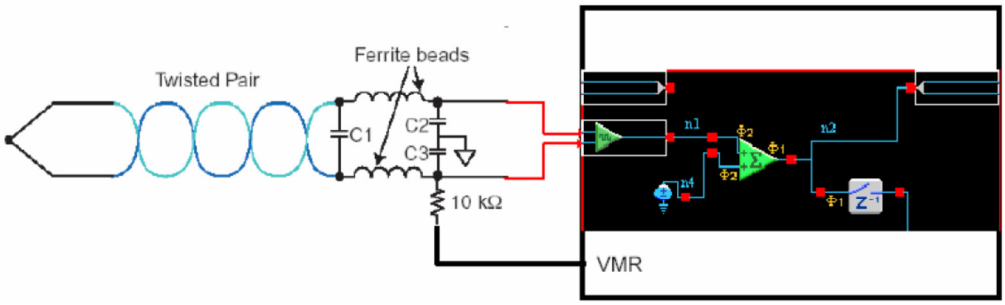


Figure 3.37 Thermocouple connected to FPAA for sensor signal processing.

STRAIN GAUGE

Strain gauge has typical output voltage of 10 mV/V. Half bridge configuration has strain gauges in two arms, which doubles the output and compensates for thermal effects. Full bridge has strain gauges in four arms and re-doubles output and also compensates for thermal effects. Figure 3.38 shows an example for processing the signal provided by a strain gauge sensor.

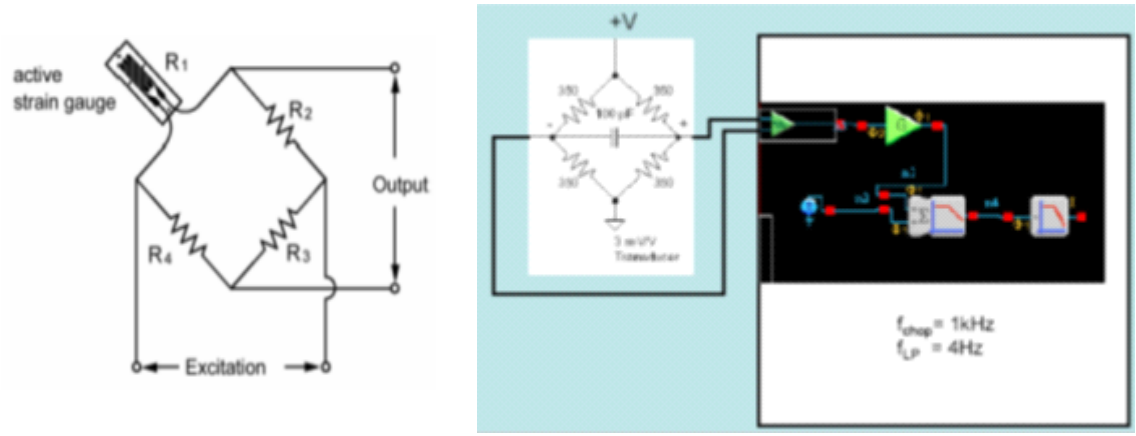


Figure 3.38 Strain gauges connected to FPAA for sensor signal processing [32].

LVDT

Linear voltage differential transformer (LVDT), has the following sensitivity ranges:

- 0.05 mV/V/0.001 for long stroke LVDTs.
- 10 mV/V/0.001 for short stroke LVDTs.

Figure 3.39 shows the sensor connection example.

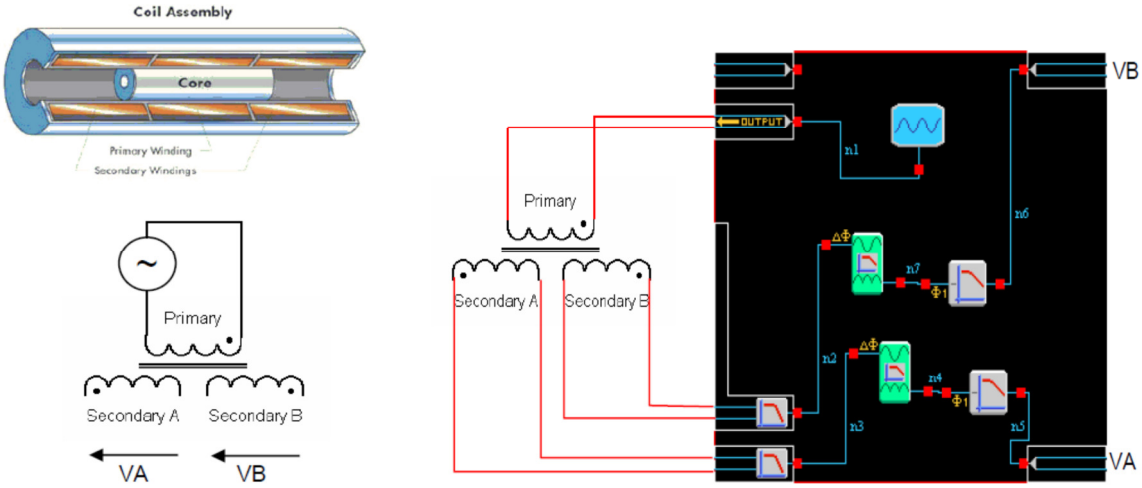


Figure 3.39 LVDT connected to FPAA for sensor signal processing [32].

HALL EFFECT DEVICES

Hall effect sensor is usually driven with a constant current and has differential output voltage, superimposed on a common-mode voltage approximately equal to half the excitation voltage.

Typical sensitivity is:

- 1-100 mV/kG.
- Refrigerator magnet of 200 gauss.

Typical element resistance:

- 1 to 10 Ω

Typical excitation current:

- 20 to 200 mA.

Typical linearity:

- 0.1% to 2%.

Figure 3.40 shows the sensor connection example.

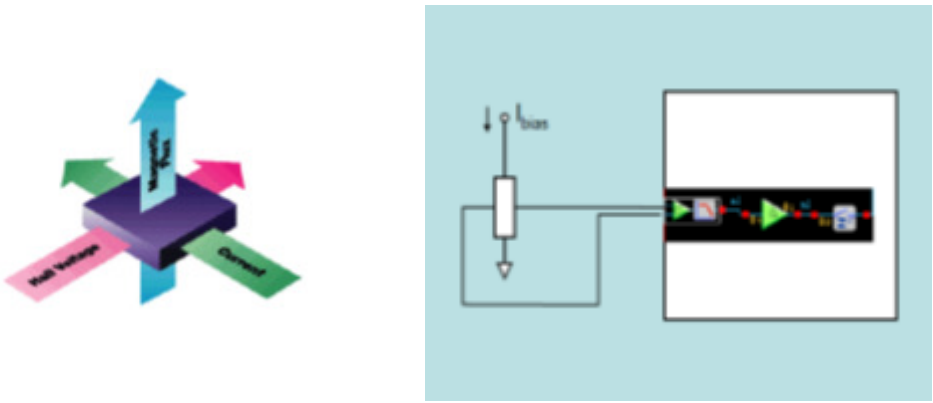


Figure 3.40 Hall effect sensor connected to FPAA for signal processing [32].

SENSOR LINEARIZATION

An important feature of the FPAA, is the use of transfer function CAM that provides the chance to linearize the output for a non-linear sensor input as occurs with the NTC thermistor. Figure 3.41 shows the connection of NTC thermistor with non-linear characteristics and the FPAA transfer function CAM should provide processing data treatment for a linear characteristic temperature versus voltage output. The CAM transfer function should be parameterized with the conversion table (LUT).

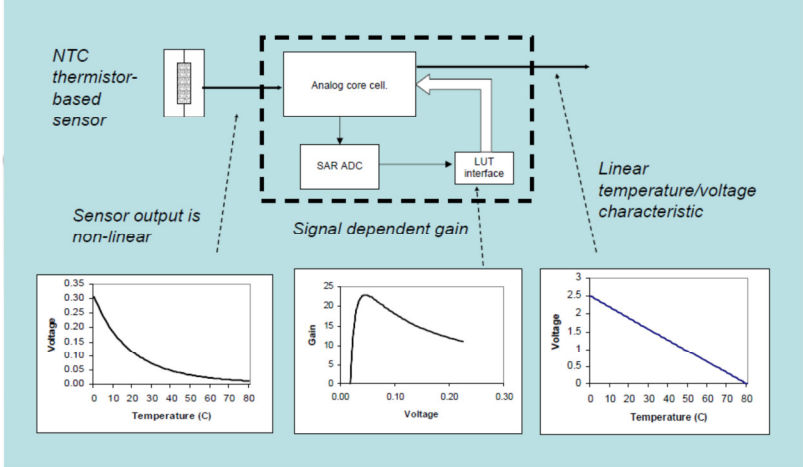


Figure 3.41 NTC thermistor with non-linear characteristics and the FPAA block output with a linear characteristic temperature versus voltage [32].

3.4 APPLICATIONS USING FPAAS

As mentioned already, it is necessary to do I/O interface of external analog signals to Input channels or Output channels of dpASP. Next topics will mention the hardware implementation of such circuits. The first one will be used for signal conditioning, connecting to the differential input channel of dpASP. The second circuit is responsible to convert differential signal provided by output of dpASP, and getting single-end signal that could be used to drive an actuator.

Also, it is implemented experiments with first order and second order transfer functions programed on AnadigmDesigner, and after simulation, downloaded to development board. The results from simulator will be compared with the measured results with oscilloscope.

3.4.1 INPUT INTERFACE CIRCUIT

This circuit uses a TL081 OPAMP which input is connected to analog signal provided by sensor or other signal to be processed by dpASP/FPAA. The output makes level-shift to VMR voltage and is connected to dpASP/FPAA differential input. The input to this circuit is single-end since inverted input pin 2 is connected to ground. Figure 3.42 shows the circuit schematic.

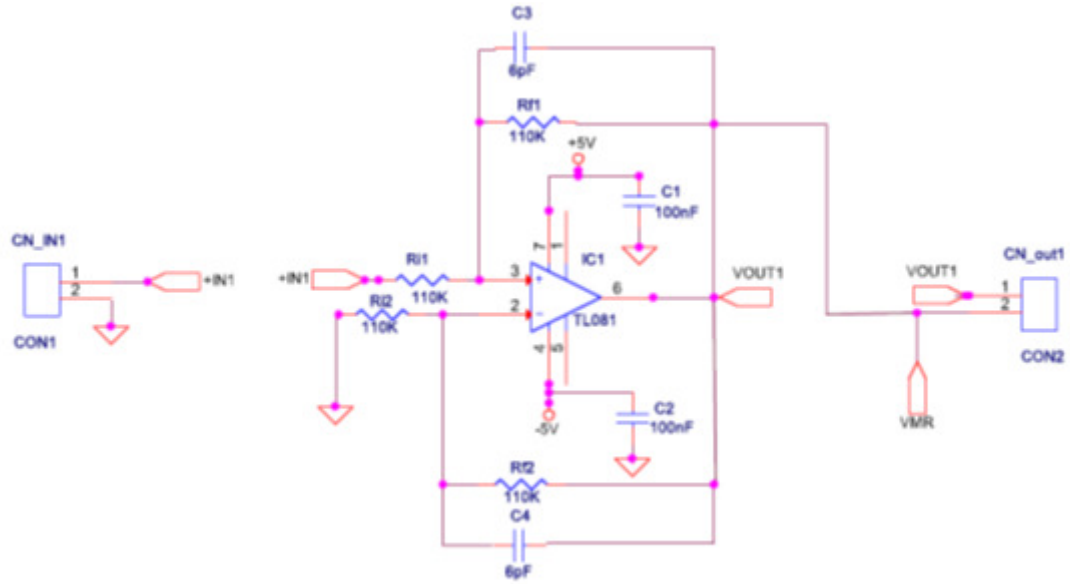


Figure 3.42 Base circuit of input interface board.

VMR voltage of 1.5 V is provided by FPAA board. Feedback capacitors C3 and C4 make the noise filtering and his value of 6 pF was fixed by experiments done with oscilloscope.

The input interface board design on Appendix A, has available four of these circuits.

3.4.2 OUTPUT INTERFACE CIRCUIT

The device Output is differential and is converted to single-ended and signal level-shifted. It uses the AD8130 which is a differential IN single-ended OUT OPAMP with a reference voltage input. The gain of this circuit can be modified by adjusting the values of the resistor RF1. Using differential amplifiers has the advantages of handle signals referenced to

any voltage, signals of any amplitude, and differential or single-ended signals. Figure 3.43 shows the circuit schematic.

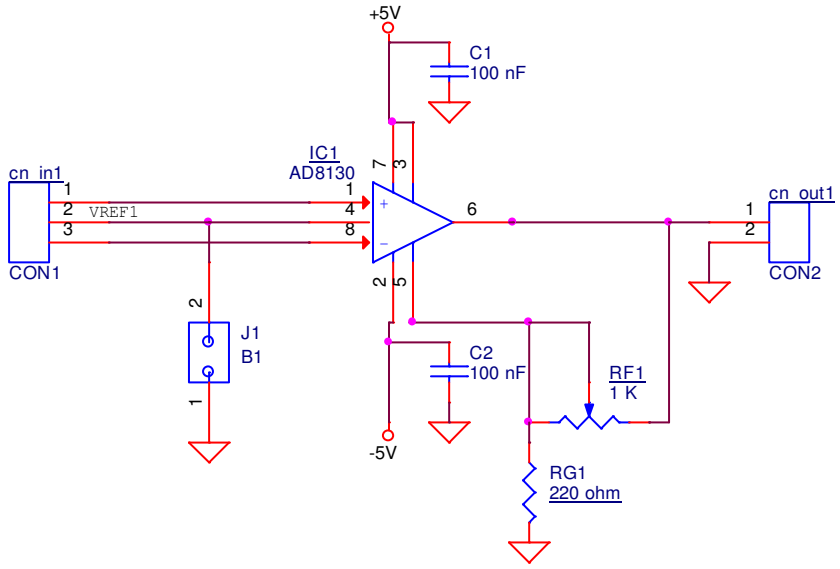


Figure 3.43 Base circuit of output interface board.

VREF1 should be connected to the ground using the jumper J1, peak voltage from cn_out1 is 5 V according to the board power supply.

The output interface board design on Appendix B, has available four of these circuits.

3.4.3 TRANSFER FUNCTION APPLICATION EXPERIMENTS

To evaluate the behavior of dpASP regarding transfer function implementation, it is used several CAMs available on AnalogDesigner 2.

FIRST ORDER, BILINEAR TRANSFER FUNCTION

It is used the bilinear filter CAM, that creates a single pole, in a low pass configuration. The filter has programmable corner frequency of 400 Hz and it is connected an input signal with 100 Hz (square wave) from a generator.

The transfer function for this circuit is:

$$\frac{Vout(s)}{Vin(s)} = \pm\frac{2\pi f_0 G}{s+2\pi f_0} \tag{3.4}$$

The pass-band gain is G and the corner frequency f_0 is the frequency at which the gain is -3+20log(G) dB. The circuit realized by the CAM is shown in Figure 3.44, in non-inverting configuration, Clock A has frequency of 250 kHz. Input sampling is done on phase 1. However, switch phasing is dependent on CAM options.

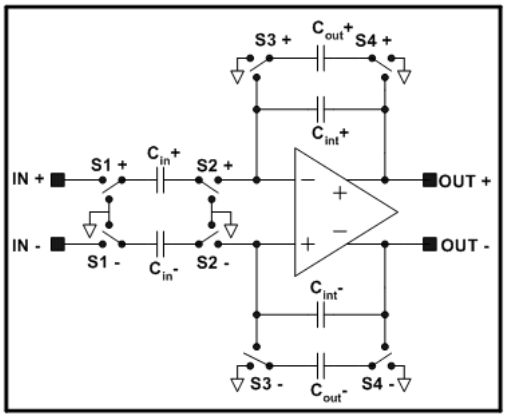


Figure 3.44 Hardware circuit implemented on dpASP.

The circuit designed and CAM configuration is shown in Figure 3.45.

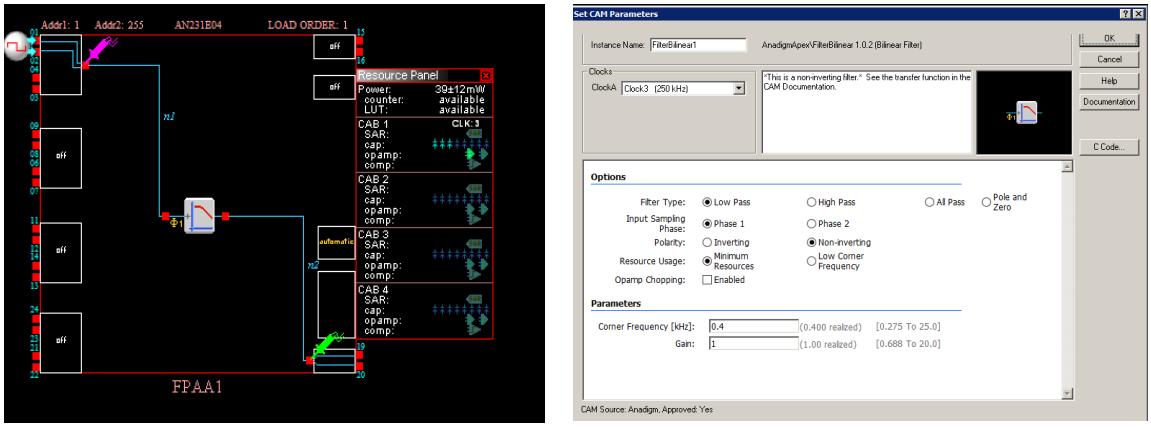


Figure 3.45 Circuit designed and configuration.

The time response on simulator is shown in Figure 3.46 by the green probe, where it is possible to see the step response on each period of the input square wave to the first order transfer function.

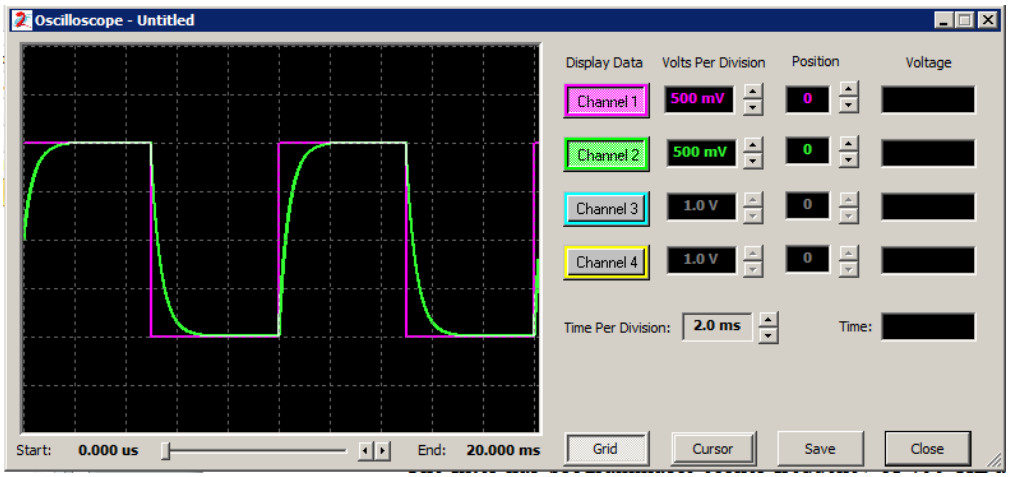


Figure 3.46 Bilinear filter, first order time response.

Figure 3.47 shows the corresponding response time obtained with oscilloscope, programming the bilinear CAM on the dpASP.

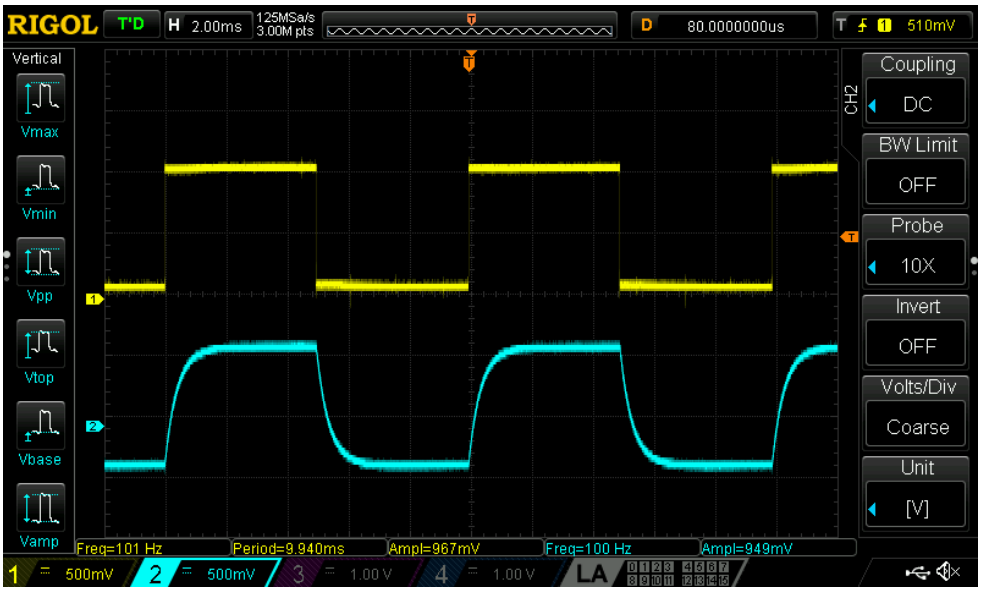


Figure 3.47 Bilinear filter, first order time response on digital oscilloscope.

The low pass bilinear filter could also be configured in pole/zero form, as shown by the following equations:

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{G_H(s + 2\pi f_z)}{s + 2\pi f_p}$$
$$G_L = G_H \frac{f_z}{f_p} \tag{3.5}$$

G_L is the DC gain, G_H is the high frequency gain, f_p is the pole frequency, and f_z is the zero frequency. The zero frequency may be higher or lower than the pole frequency.

The circuit is presented in Figure 3.48.

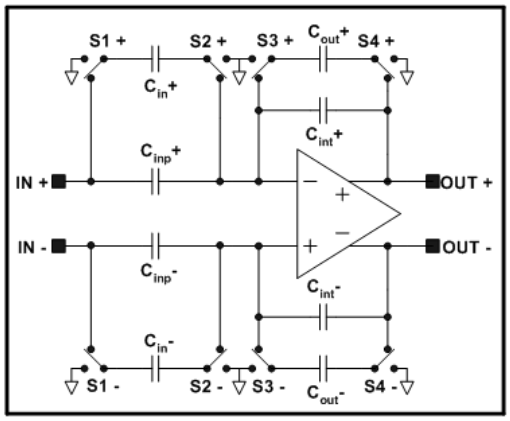


Figure 3.48 Bilinear filter, zero/pole form.

SECOND ORDER, BIQUADRATIC TRANSFER FUNCTION

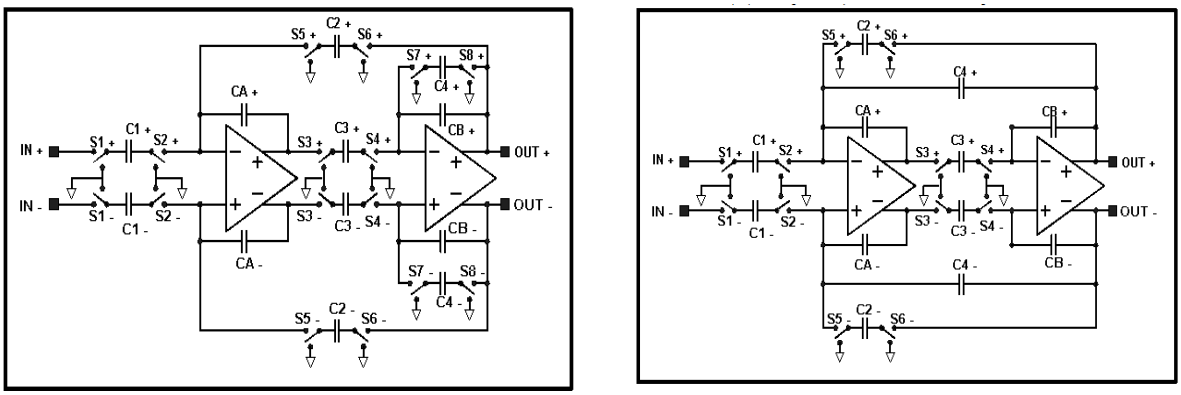
This CAM creates a full cycle, biquadratic (two pole) low pass filter, it has programmable corner frequency of 500 Hz, unit pass band gain, and quality factor Q = 2.5.

The transfer function for this circuit is:

$$\frac{V_{Out}(s)}{V_{In}(s)} = \frac{\pm 4\pi^2 \times {f_0}^2 \times G}{s^2 + \frac{2\pi \times f_0}{Q} s + 4\pi^2 \times {f_0}^2} \tag{3.6}$$

G is the pass-band gain (DC gain), f_0 is the corner frequency, and Q is the quality factor.

Two different circuits can realize the low pass version of the biquadratic filter. The implementation that best fits the combination of CAM parameter values is automatic selected. Figure 3.49 shows the first circuit on left side and second circuit on right side.



a) b)

Figure 3.49 Automatic selection done by AnadigmDesigner 2: a) first circuit configuration; b) second circuit configuration.

The circuit designed and CAM configuration is shown in Figure 3.50.

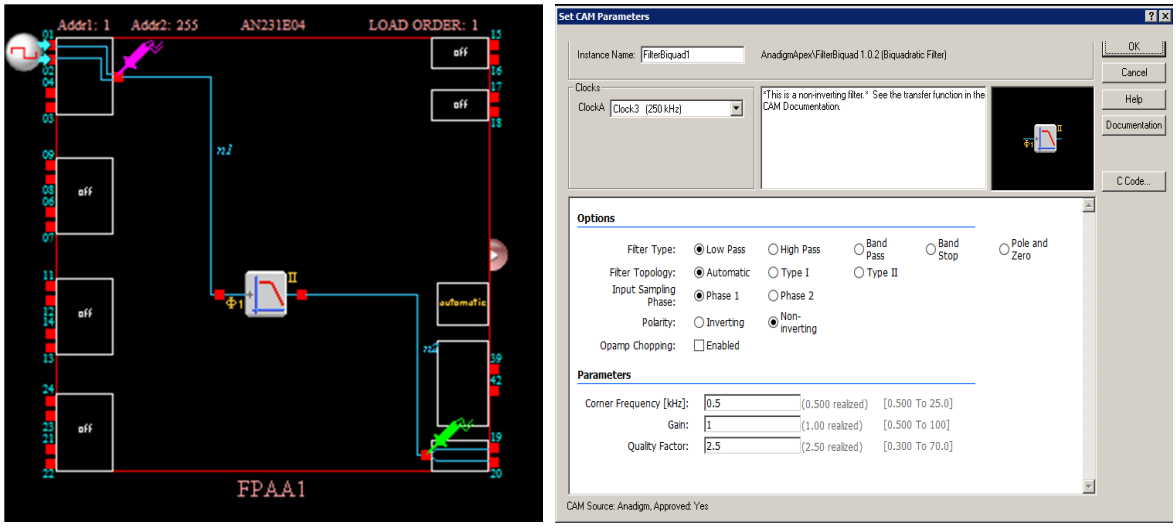


Figure 3.50 Circuit designed and configuration settings.

The time response on simulator is shown in Figure 3.51 by the green probe, where it is possible to see the step response on each transition voltage level of input square wave.

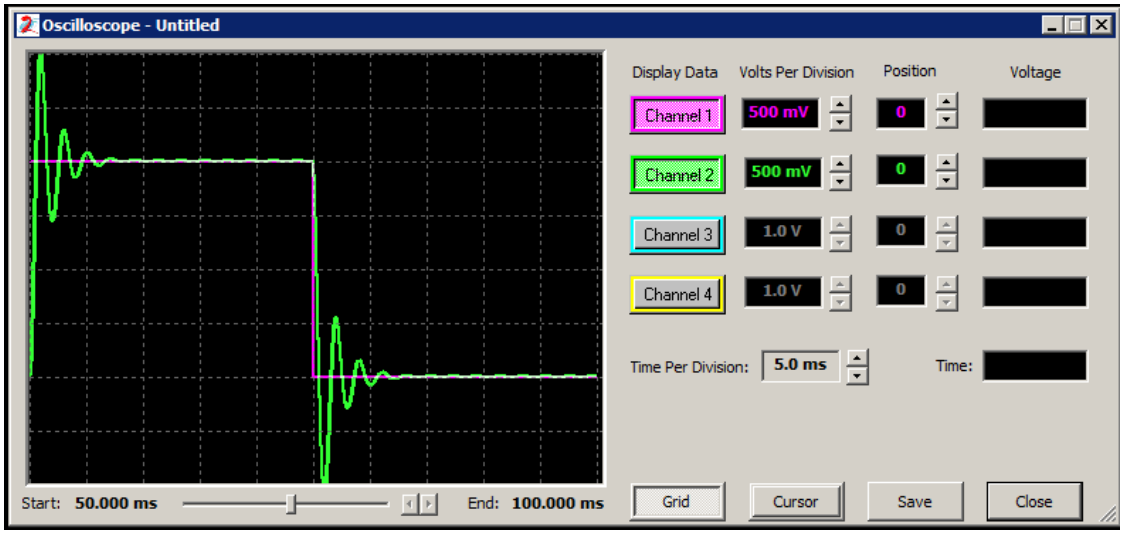


Figure 3.51 Biquadratic filter, second order system response.

Figure 3.52 shows the corresponding response time obtained with oscilloscope, programming the biquadratic CAM on the dpASP.

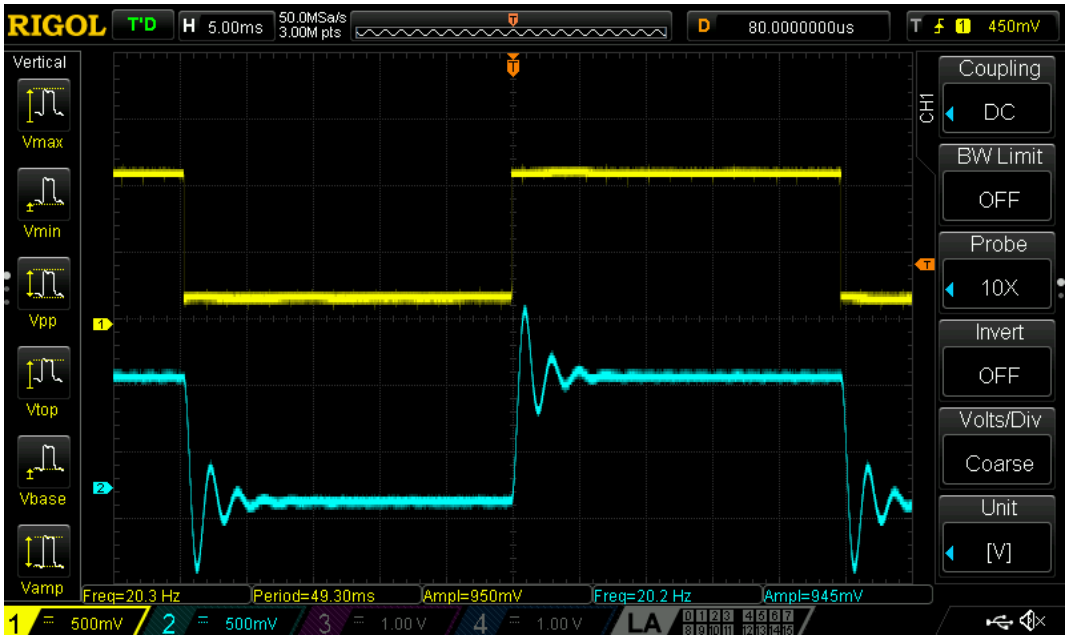


Figure 3.52 Biquadratic filter, first order time response on digital oscilloscope.

Pole and zero biquadratic Filter is also possible, as shows the following equation for transfer function:

$$\frac{V_{Out}(s)}{V_{In}(s)} = -\frac{G_H \times \left(s^2 + \frac{2\pi \times f_Z}{Q_Z} s + 4\pi^2 \times {f_Z}^2\right)}{s^2 + \frac{2\pi \times f_P}{Q_P} s + 4\pi^2 \times {f_P}^2} \tag{3.6}$$

G_L, the DC gain, is a function of the pole and zero frequencies and high frequency gain and may cause clipping when high:

$$G_L = G_H \left(\frac{f_z}{f_p}\right)^2 \tag{3.7}$$

Figure 3.53 shows the internal dpASP circuit configuration.

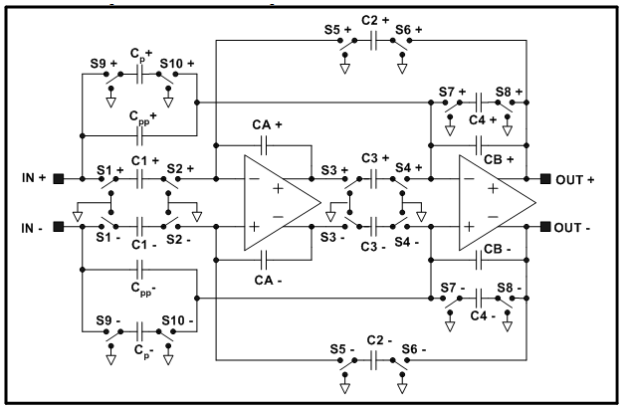


Figure 3.53 Biquadratic filter, zero/pole form.

HIGH ORDER TRANSFER FUNCTION

Transfer function of high order can be mathematically described using high-order polynomial expressions. Such expressions can be re-written as products of simpler ones, where the numerator and denominator are up to first order bilinear expressions or second order biquadratic expressions. Figure 3.54 shows a cascade design of a bilinear filter followed by two biquadratic filters. This configuration implements a fifth order transfer function.

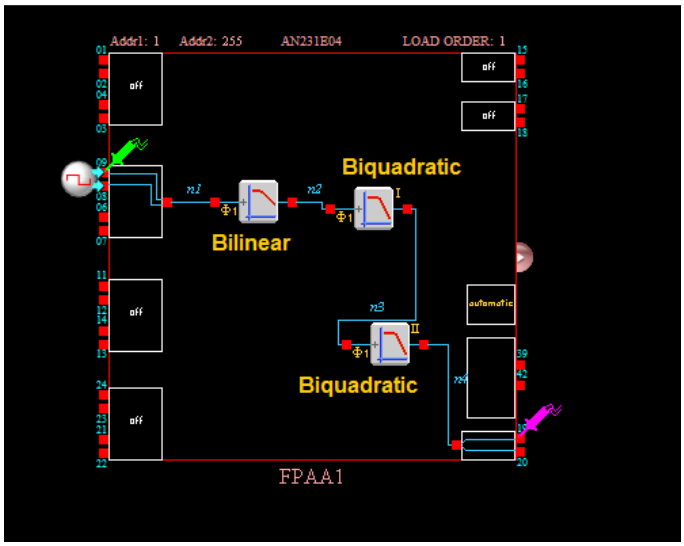


Figure 3.54 Fifth order filter design.

The step response is shown in Figure 3.55 by the green probe of Anadigm designer simulator.

Figure 3.55 Fifth order filter , step response on simulator.

Figure 3.56 shows the related response time obtained with oscilloscope, programming the cascade circuit with a bilinear CAM, followed by two biquadratic CAMs on the dpASP.

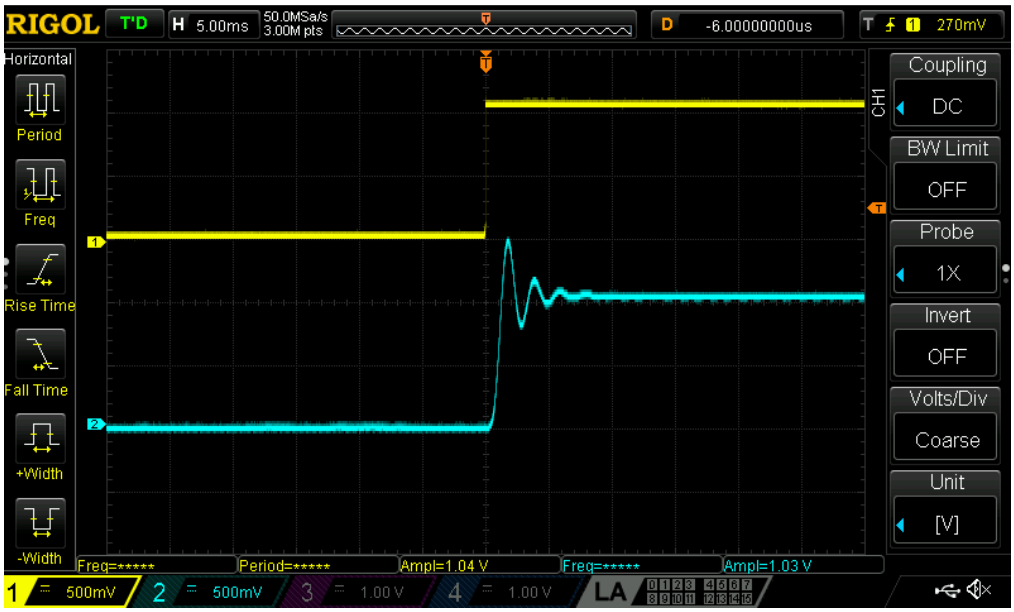


Figure 3.56 Fifth order filter, step response on oscilloscope.

Also, higher order transfer functions can be designed in AnadigmFilter tool, using as examples Butterworth, Chebyshev and Bessel filters.

DELAY TRANSFER FUNCTION

There are plant processes that have a lag on response to the unit step function. To simulate this behavior is possible to implement a delay CAM function as shows Figure 3.57. In terms of time domain, this means that the input is passed unchanged to the output after the specified programmed delay. The realized transfer function is the exponential function as follows:

$$G(s) = e^{-Ls} \tag{3.8}$$

Where, L is the programmed time delay parameter of the CAM. For the following example, L has the value of 200 ms.

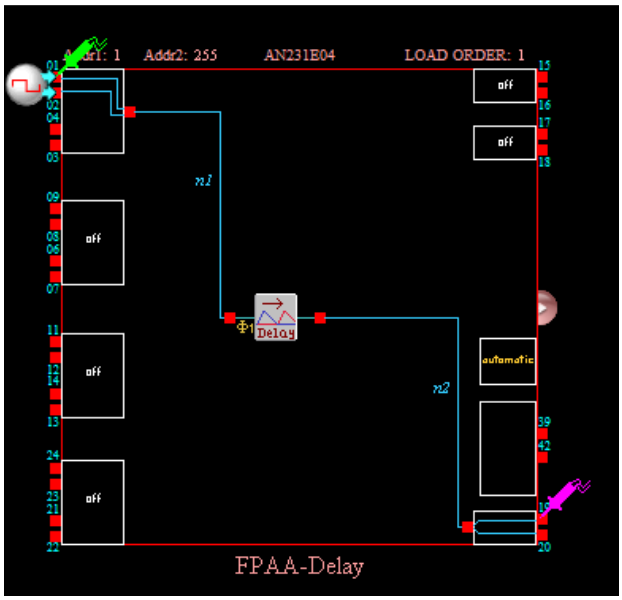


Figure 3.57 Delay transfer function.

The step response is shown in Figure 3.58 by the pink probe of AnadigmDesigner simulator.

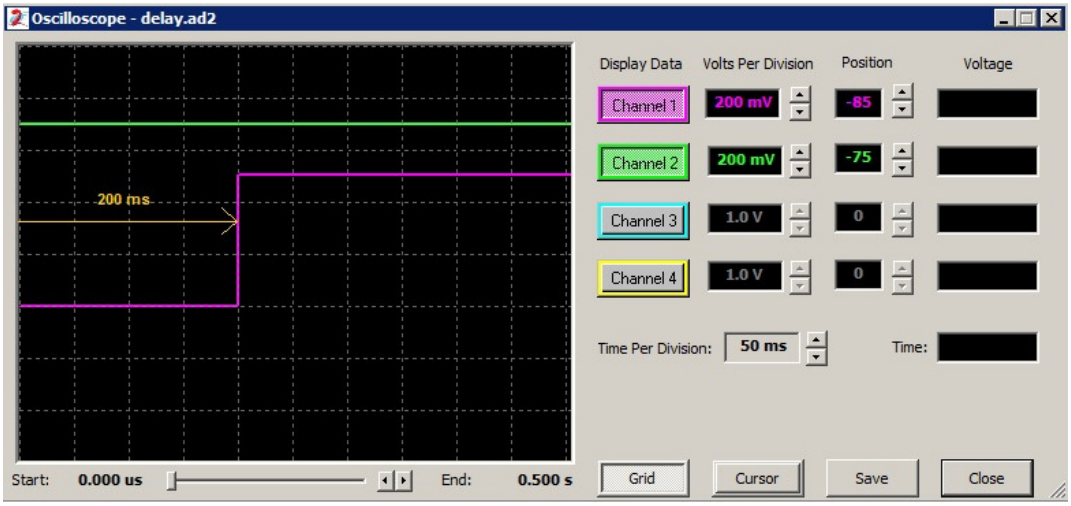


Figure 3.58 Delay step response on simulator.

Figure 3.59 shows the related time response obtained on oscilloscope.

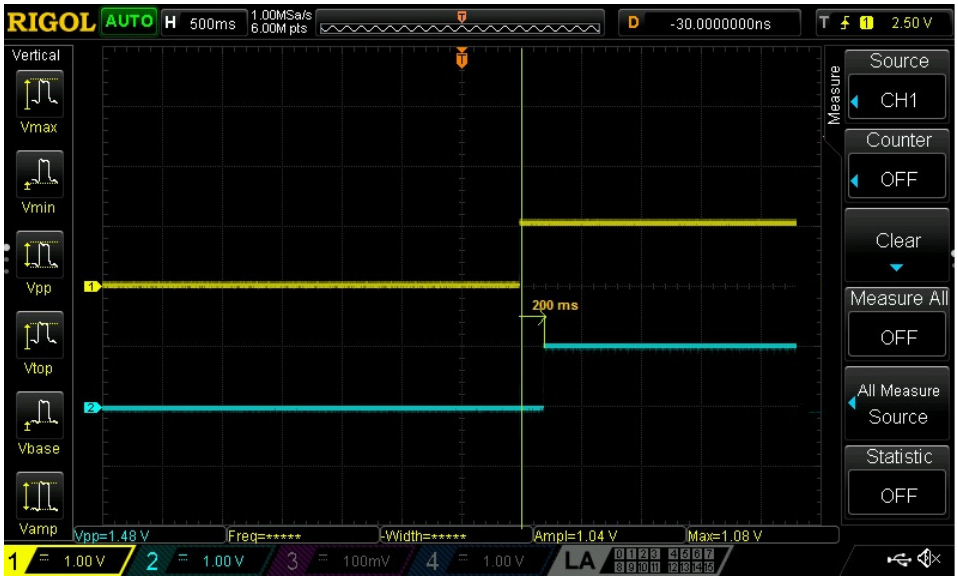


Figure 3.59 Delay step response on oscilloscope.

FIRST ORDER TRANSFER FUNCTION WITH LAG

As mentioned on previous example, the lag response of transfer function applied to step response occurs on some plant processes, especially on physical processes which can be in most of cases simulated by a first order transfer function with lag response. As example, the temperature control inside a chamber or room.

Figure 3.60 shows the circuit programmed on FPAA that implements the first order transfer function with lag response to the unit step input function.

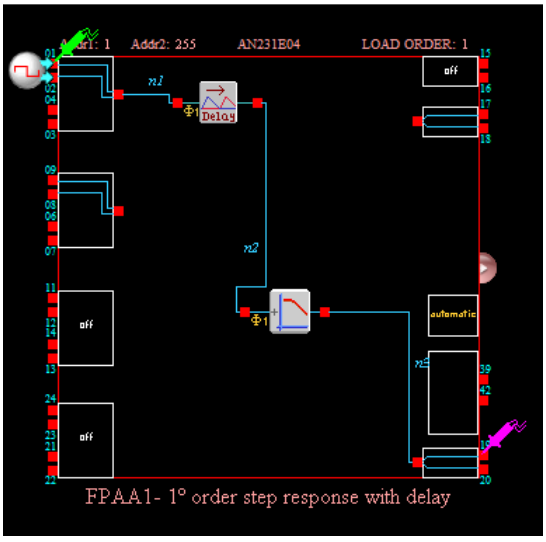


Figure 3.60 First order transfer function with lag response.

The step response is shown in Figure 3.61 by the pink probe of Anadigm designer simulator. The delay of response is 200 ms.

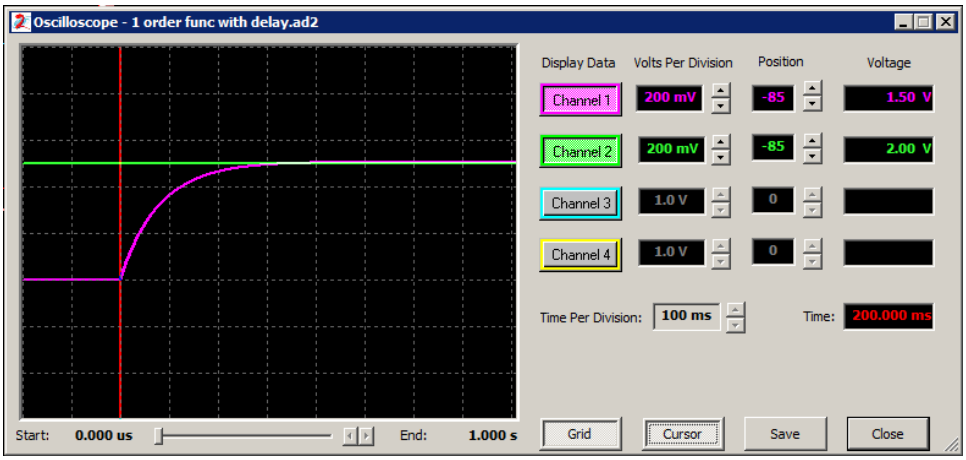


Figure 3.61 Step response of first order transfer function with delay on simulator.

Figure 3.62 shows the corresponding time response obtained on oscilloscope.

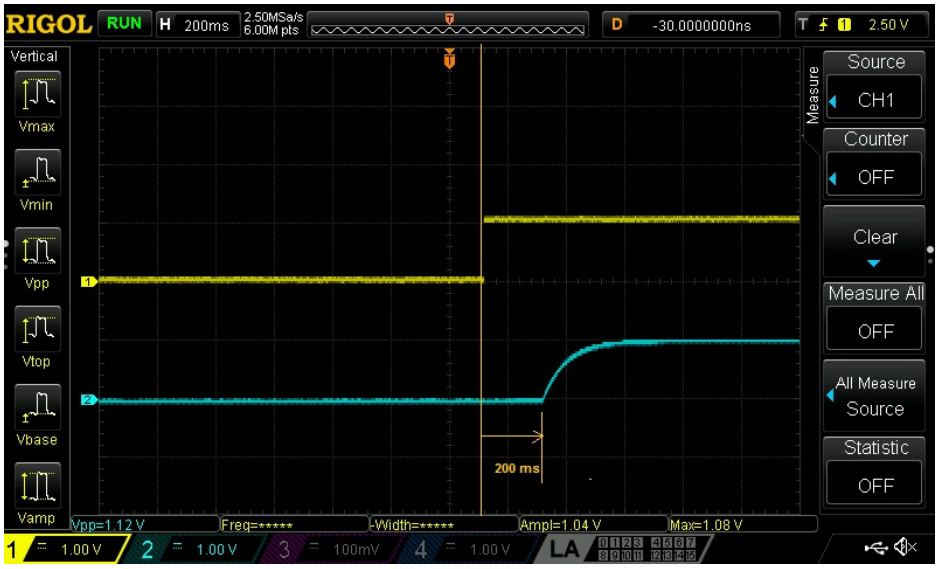


Figure 3.62 Step response of first order transfer function with delay on oscilloscope.

Chapter 4 will focus in detail the transfer functions of several physical systems representing the plant processes as well the configuration of FPAA/dpASP to implement PID controller applied to control a process.

3.5 DISCUSSION

This chapter described the FPAA/dpASP development hardware from Anadigm as well several methods to interface input pins to make signal conditioning for sensors. To make the interface to the I/O pins of FPAA/dpASP it should be designed circuits based on AMPOPs or use only in case of input channels the Rauch Filter with passive components that should be calculated taking into consideration the gain , quality factor and corner frequency.

It was necessary to make lot of experiences in laboratory to achieve the final design of the input interface board circuit based on AMPOP TL081 due to noise filtering. To solve the problem, it was implemented, after several trials, capacitors of 6 pF in parallel with RF1 and RF2 feedback resistors that gave the best response to avoid overshoots in the dpASP input.

For to the output interface board circuit design, it was implemented a differential receiver to convert the signal end IC from Analog Devices, AD8130. This IC has high bandwidth with programmable gain and was able to avoid distortion on output. Also converts the reference internal VMR from dpASP to the GND reference to be able to drive external circuits that normally are referenced to the ground. It was tested the AMPOP TL081 for the output interface circuit but the results were not so good as comparing with the ones obtained with AD8130, due to occurrence of higher distortion and instability for output signals of same frequency.

Finally, it was implemented transfer functions of several orders on dpASP/FPAA using CAM filter circuits. To perform these tests, it was used a function generator to send the step signal or square wave with low frequency to the input interface circuit which output is connected to the input channel of dpASP. The input from output interface circuit board was connected to differential output channel from dpASP and output of output interface circuit was connected to oscilloscope. The obtained results with oscilloscope were very similar with ones obtained with Anadigm simulator.

These experiments were very important to validate the concept design of input and output interface circuitry boards and as well to test the simulation of transfer functions using CAM design implementation on the FPAA/dpASP hardware.

4 SYSTEM CONTROL DESIGN FOR FPAA

In previous chapter, it was discussed the FPAA technologies and applications, based on Anadigm Corporation hardware and software. This chapter will focus the FPAA in terms of system control implementation of PID control. It should be noted that more than 90% of the industrial controllers in use today utilize PID based control. Because, most PID controllers are adjusted on-site, many different types of tuning methods have been proposed in literature. Using these tuning methods, fine tuning of PID controllers can be made on-site much easier. Also, PID controls are in general applicable to most control systems. In particular, when the mathematical model of the plant is not known and therefore analytical design methods cannot be used, PID controls prove to be most useful.

This chapter describes the design concept and tuning methods of PID controlled systems and application of PID design model to FPAA/dpASP hardware technology. It is described the implementation of PID controller on Anadigm third generation dpASP using CAMs library of AnadigmDesigner2 and several technics to avoid noise propagation on the circuit.

4.1 TUNING METHODS FOR PID CONTROLLER

A plant with a mathematical model defined can be used to apply various design techniques to determine parameters of the controller that will meet the transient and steady-state specifications of the closed-loop system. However, if the plant is so complicated that its mathematical model cannot be easily obtained, then an analytical approach to the design of PID controller is not possible. In this case, it could be used experimental approaches to the tuning of PID controllers [36].

The PID controller can be implemented using analog circuits, software (discrete PID controller algorithm made in Assembly or C/C++) with microcontrollers or PLD/FPGAs (Discrete PID controller implemented on hardware inside chip using VHDL/VERILOG language).

All implementations have advantages and disadvantages:

- The classical analog implementation has the advantages of continuously operation of algorithm calculations made on continuous time domain, but it is difficult to tune the constants. This process should be done manually and is time consuming.

- Software implementation of the PID controller presents advantage of easily tuning and adjusting the controller parameters, with the possibility for auto-tuning or self-tuning. This implementation is more flexible, but it has disadvantages as treatment of signals with microcontroller resources are mostly used for PID algorithm than for other tasks. Also, there are some difficulties for fast time response applications and algorithm calculations made on discrete time domain.

- PLD/FPGAs implementation has advantages of implementation in physical hardware on chip using VHDL/VERILOG languages, easy re-configurability of PID. Disadvantage of implement filters to mitigate noise and anti-aliasing. Also algorithm calculations are made on discrete time domain.

With appearance of FPAA/dpASP, the PID controller is implemented in the analog continuous time domain, with possibility of easily reconfiguration and even auto-tuning of the controller parameters, reducing time for setting and increasing the flexibility. Easy

programming application on AnadigmDesigner 2 with internal tool simulator where is possible to check the wave shapes before download the design to the hardware.

Taking into consideration the mentioned characteristics of dpASP/FPAAs, PID mathematical model and calculations will be made using Laplace *s* continuous time domain.

The ideal transfer function for the PID controller in continuous time domain can be expressed as:

$$u(t) = K_p.e(t) + K_i \int_0^t e(\tau)d\tau + K_d \frac{de(t)}{dt} \tag{4.1}$$

The transfer function of a PID controller on *s* continuous domain is obtained applying Laplace transform of previous equation. The following two equivalent equations are the transfer function of PID controller:

$$G_c(s) = \frac{U(s)}{E(s)} = K_p \left[1 + \frac{1}{T_i s} + T_d s\right] = K_p + \frac{K_i}{s} + K_d s \tag{4.2}$$

where $K_i = \frac{K_p}{T_i}$ and $K_d = K_p T_d$.

Figure 4.1 shows the analog PID controller realized with operational amplifiers. The top AMPOP realizes the proportional control, the middle AMPOP circuit realizes the integration function control and the bottom AMPOP circuit realizes the differential function control.

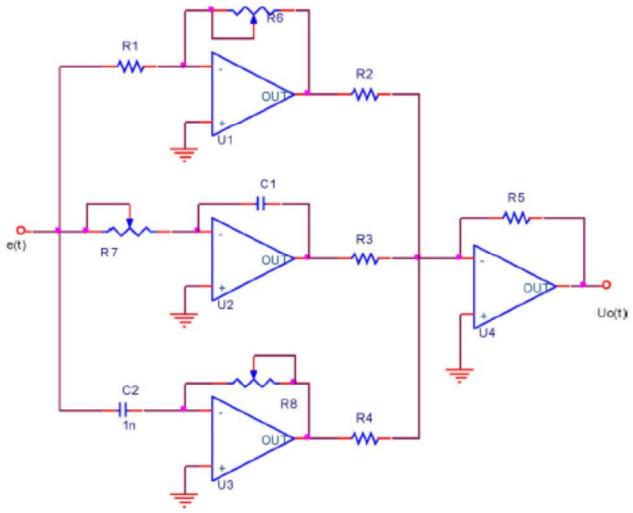


Figure 4.1 Analog PID controller with AMPOPs [38].

Figure 4.2 shows the PID controller equation block and process plant in a feedback closed-loop control system.

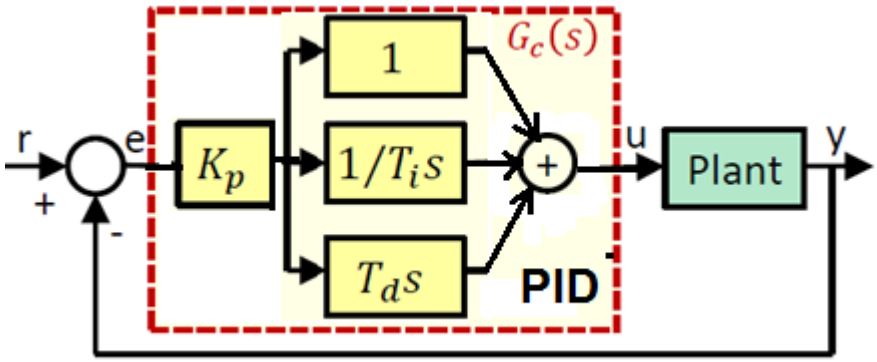


Figure 4.2 PID control of a plant.

The process of selecting the controller parameters to meet given performance specifications is known as controller tuning. Several methods and equations to get control initial parameters were developed, for instance by:

- J. G. Ziegler and N. B. Nichols (1942, 1943).
- Shinskey (1979).
- Cohen and Coon (1953).

However, there are more tuning methods available which can be found on book "Handbook of PI and PID controller tunning rules, 2nd edition, Imperial College press" from Mr. Aidan O´Dwyer.

This chapter is focus on approach presented by J. G. Ziegler and N. B. Nichols that recognized step responses of a large number of process control systems exhibit a process reaction curve with S-shape. Ziegler and Nichols suggested rules or methods for tuning PID controllers based on experimental step responses of the process dynamics. Ziegler-Nichols methods are also useful when mathematical models of plants are not known. These methods can, of course, also be applied to the design of systems with known mathematical models. The methods suggest a set of values of K_p, T_i and T_d, that will give a stable operation of the system. However, the resulting system may exhibit a large maximum overshoot in the step response,

which is unacceptable. In such a case it is necessary to perform series of fine tunings until an acceptable result is obtained. In fact, the Ziegler-Nichols tuning methods provide initial parameter values and it is a starting point for fine tuning, rather than giving the final settings for K_p, T_i and T_d of a PID controller.

4.1.1 First Method For Tuning PID Controller

In the first method, we obtain experimentally the response of plant to a unit-step input in open loop. If the plant does not involve integrator(s) or dominant complex-conjugate poles, then a unit-step response curve may look S-shaped, as shown in Figure 4.3. In fact, this method applies if the response to a step input exhibits an S-shaped curve and such step-response curves may be generated experimentally or from a dynamic simulation of plant.

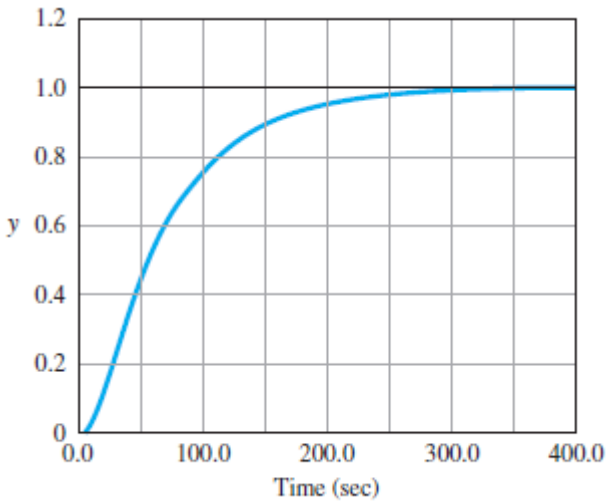


Figure 4.3 Step response of plant [37].

The S-shaped is a first-order system with a time delay of L = t_d . The constants can be determined from the unit step response of the process. If a tangent is drawn at the inflection point of the reaction curve, then the slope of the line is R = A/τ and the intersection of the tangent line with the time axis identifies the time delay L = t_d, as shown in Figure 4.4.

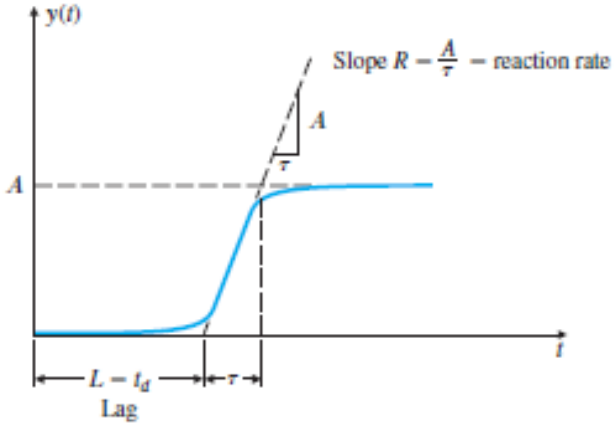


Figure 4.4 Plant response to the unit step [37].

The transfer function Y(s)/U(s), approximated first-order system with a transport lag as following equation:

$$\frac{Y(s)}{U(s)} = \frac{Ae^{-st_d}}{\tau\, s + 1} \tag{4.3}$$

Ziegler and Nichols suggested to set the values of K_p, T_i and T_d according the controller type using formulas shown in Table 4.1 and considering the PID transfer function as follows:

$$G(s) = K_p\left[1 + \frac{1}{T_i s} + T_d s\right] \tag{4.4}$$

Table 4.1 Gain parameter values according first method of Ziegler-Nichols [37].

Type of Controller	K_p	T_i	T_d
P	$\frac{1}{RL}$	∞	0
PI	$\frac{0.9}{RL}$	$\frac{L}{0.3}$	0
PID	$\frac{1.2}{RL}$	$2L$	0.5L

The controller parameters are designed to result in a closed-loop step response transient with a decay ratio of approximately 0.25. This means that the transient decays to a quarter of its value after one period of oscillation as shown in Figure 4.5. A quarter decay corresponds to $\zeta = 0.21$ and is a reasonable compromise between quick response and adequate stability margins.

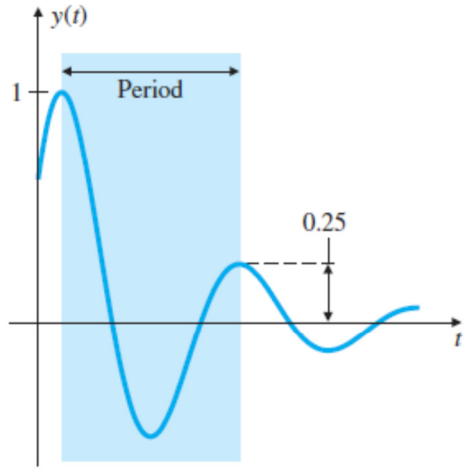


Figure 4.5 Closed-loop plant response to the unit step input [37].

4.1.2 SECOND METHOD FOR TUNING PID CONTROLLER

On second method, the ultimate sensitivity method, the criteria for adjusting the parameters are based on evaluating the amplitude and frequency of the oscillations of the system at the limit of stability rather than on taking a step response. To use the method, the proportional gain is increased until the system becomes marginally stable and continuous oscillations just begin, with amplitude limited by the saturation of the actuator (Figure 4.6). The corresponding gain is defined as K_u (called the ultimate gain) and the period of oscillation is P_u (called the ultimate period). P_u should be measured when the amplitude of oscillation is as small as possible. Then the tuning parameters are selected as shown in Table 4.2.

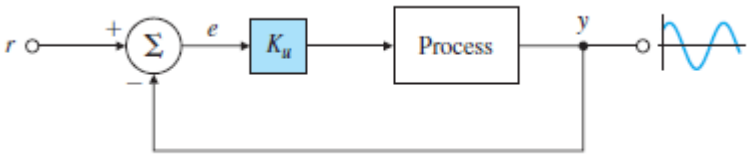


Figure 4.6 Determination of the ultimate gain and period [37].

The critical gain K_u, and the corresponding period P_u, are experimentally determined using Figure 4.7.

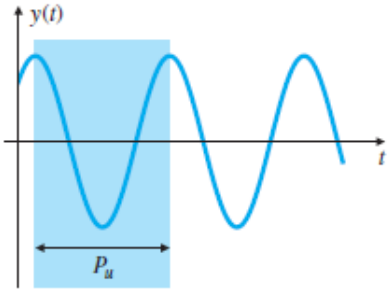


Figure 4.7 Determination of critical period [37].

Ziegler and Nichols suggested setting the values of the parameters K_p, T_i and T_d according to the formulas shown in Table 4.2, which are based also on equation (4.4).

Table 4.2 Gain parameter values according second method of Ziegler Nichols [37].

Type of Controller	K_p	T_i	T_d
P	$0.5K_u$	∞	0
PI	$0.45K_u$	$\frac{P_u}{1.2}$	0
PID	$0.6K_u$	$\frac{1}{2}P_u$	$\frac{1}{8}P_u$

Experience has shown that the controller settings according to Ziegler–Nichols rules provide acceptable closed-loop response for many systems. The process operator will often do final tuning of the controller iteratively on the actual process to yield satisfactory control.

4.1.3 CHARACTERISTICS OF P, I AND D CONTROLLERS

After getting the initial parameters K_p, K_i and K_d using one of Ziegler–Nichols methods, it is necessary to optimize the system response by fine tuning. In order to perform the fine tuning it should be known the effects provided by changing each parameter.

The proportional gain (K_p) will have the effect of reducing the rise time and will reduce but never eliminate the steady-state error. An integral gain (K_i) will have the effect of eliminating the steady-state error, but it may make the transient response slower. A derivative gain (K_d) will have the effect of increasing the stability of the system, reducing the overshoot, and improving the transient response.

The effect of increase each gain parameters K_p, K_i and K_d on the closed-loop system are summarized in Table 4.3.

Table 4.3 Effect of parameter adjustment on closed-loop system response [37].

Closed loop response	Rise time	Overshoot	Settling time	Steady-state error	System stability
$\boldsymbol{Increase\ K_p}$	Decrease	Increase	Small change	Decrease	Degradation
$\boldsymbol{Increase\ K_i}$	Decrease	Increase	Increase	Decrease a lot	Degradation
$\boldsymbol{Increase\ K_d}$	Small change	Decrease	Decrease	No change	Improve

These correlations may not be exactly accurate, because the values K_p, K_i and K_d are dependent on each other. In fact, changing one of these variables can change the effect of the

other two. For this reason, the table should only be used as a reference when determining the control constants. Anyway, knowing the implication of changing each parameter for the fine tuning, it could be possible to improve the step system response by doing some evaluations with different values for the gain parameters, until reach the expected behavior of the controlled dynamic process system.

4.2 PID CONTROLLER DESIGN IMPLEMENTATION ON FPAAS

AnadigmDesigner2 has a specialized tool for synthesis of a PID controller. It permits the circuit configuration depending on the requirements. AnadigmPID tool is available for second generation of Anadigm FPAA/dpASPs devices but in case of third generation devices, it is not available during the time frame of this Thesis on AnadigmDesigner 2 (V2.8.0.2) released on April of 2015.

The concept of PID controller block diagram is shown on Figure 4.8. Based on it is possible to design the PID controller on third generation FPAA/dpASP, using CAM modules available on AnadigmDesigner2 CAM library.

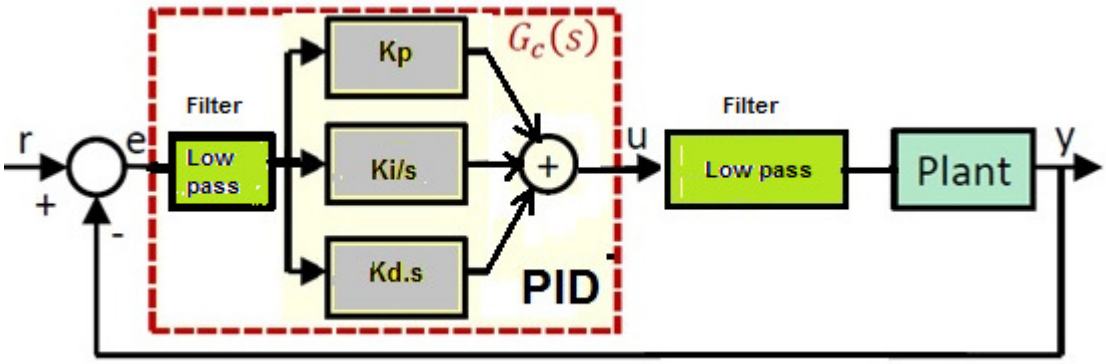


Figure 4.8 PID block model diagram.

Considering the previous figure, it should be selected specific CAMs which implement the function of each block.

The block that calculates the error based on the setpoint (SP) and the present value (PV) at plant output is designed using the half cycle sum/difference CAM as shows Figure 4.9.

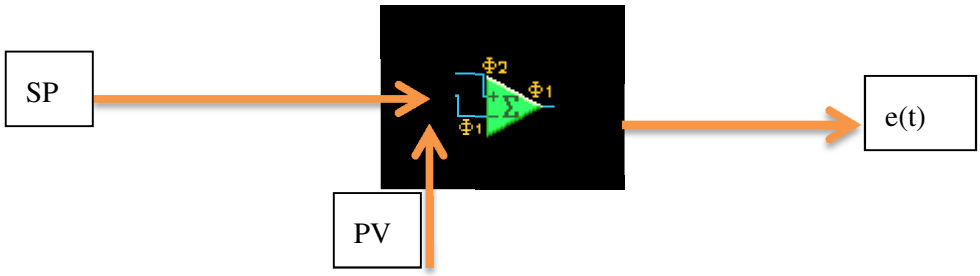


Figure 4.9 Half cycle sum/difference CAM.

The PV input should be inverted and gain equal to 1. The SP input should be non-inverted and gain equal to 1. The output signal corresponds to the error $e(t)$, difference between SP and PV on each time instant.

The proportional block could be designed using an inverting gain CAM in series with another inverting gain CAM. So, as the error input signal is inverted two times, this mean that output signal from the proportional block will have the error value multiplied by the gain value of the two gain stages in phase with the error input signal. Figure 4.10 shows the circuit diagram with two CAMs that implement the proportional block.

To increase the proportional gain K_p it should be modified the gain parameter from the first gain stage G_1 and if necessary to get a total gain value more than 100, then should be increased the gain of second gain stage G_2 to achieve the requirements.

Figure 4.10 CAM design for proportional control block implementation.

The integration block could be designed using the integrator CAM stage. The input signal is inverted as the integration control should be multiplied by the proportional control parameter that is represented by the gain stage CAM with polarity inverted. Figure 4.11 shows the CAM configuration that implements the integration block.

Integration gain K_i from the final PID controller will be gain factor from the inverted gain CAM stage G3 multiplied by the integration constant parameter g_i value.

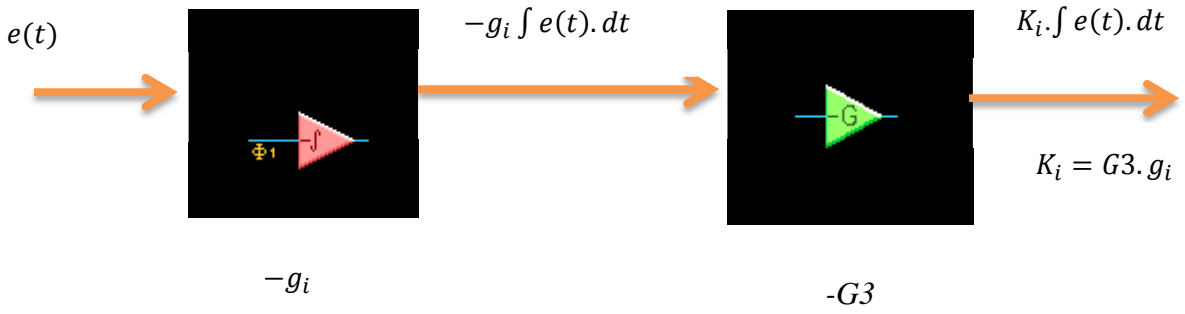


Figure 4.11 CAM design for integral control block diagram.

To evaluate the performance of integration block it is necessary to implement the design on FPAA/dpASP as shows Figure 4.12.

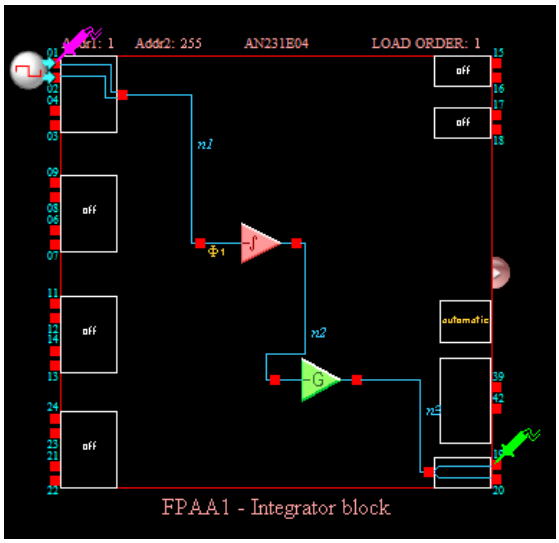


Figure 4.12 Integration block for output response validation.

The integration block setting parameters are the following ones:

- CAM clock of 20 kHz.
- Input square wave, 50 Hz, Vpp = 500 mV; duty cycle = 50%.
- Inverted integrator with integration constant, 0.2 ms.
- Inverted gain stage with gain = 1.
- Output connected to oscilloscope with 5 ms / 500 mV per division.

Figure 4.13 shows the response of integration block on simulator.

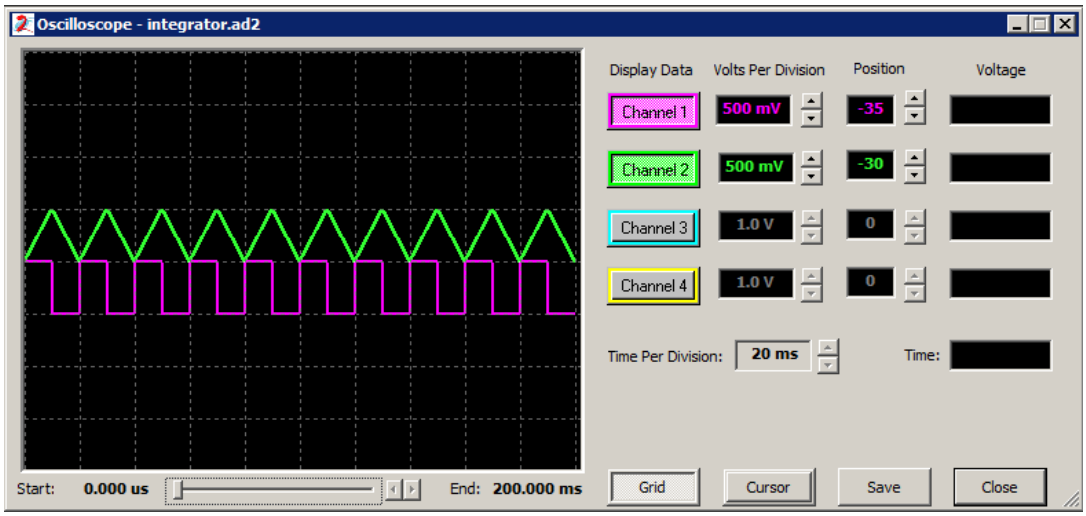


Figure 4.13 Integration block output response with square wave input on simulator.

Figure 4.14 shows the response of integration block on oscilloscope.

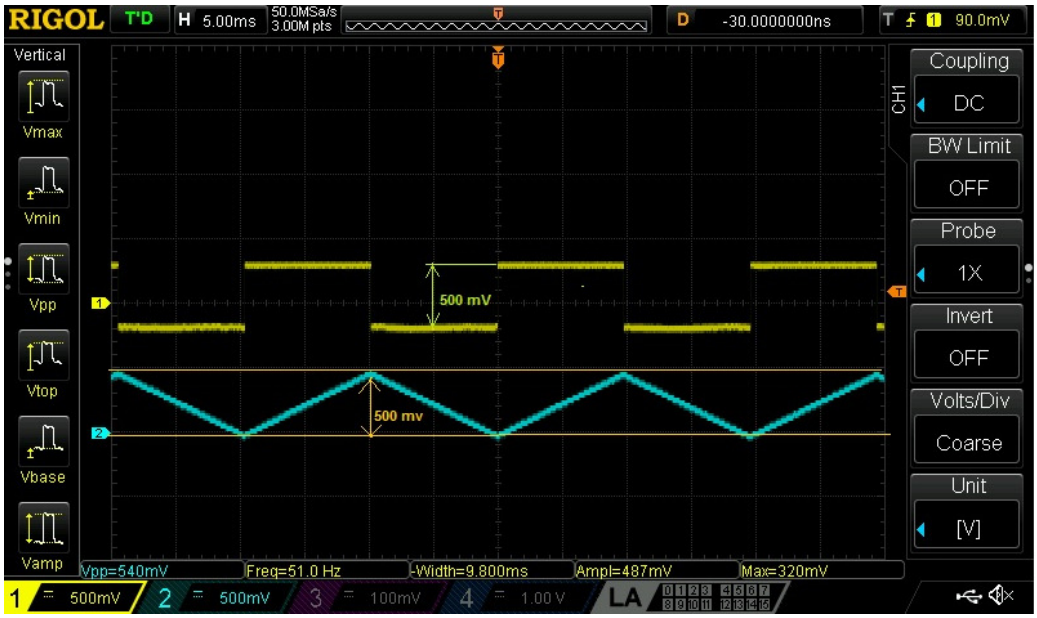


Figure 4.14 Integration block output response with square wave input on oscilloscope.

The obtained results on simulator when compared with measured wave forms on oscilloscope are very similar in terms of signal amplitudes and expected wave shapes.

The differential block can be designed using a differentiator CAM stage. The input signal is inverted to the output. The differential control should be multiplied by inverted gain parameter that is represented by the inverted gain CAM stage. Figure 4.15 shows the CAM block diagram that implements differential block.

The differential constant g_d could be adjusted by setting the differentiation constant parameter, then differential gain K_d from the PID controller will be the gain factor from the gain stage G4 multiplied by g_d value.

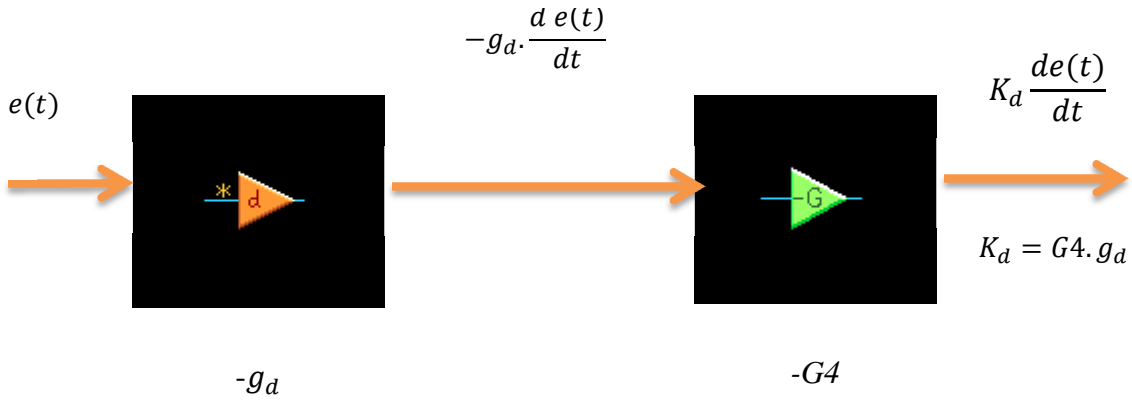


Figure 4.15 CAM design for differential control block diagram.

To evaluate the performance of differential block, it is necessary to implement the design on FPAA/dpASP as shows Figure 4.16.

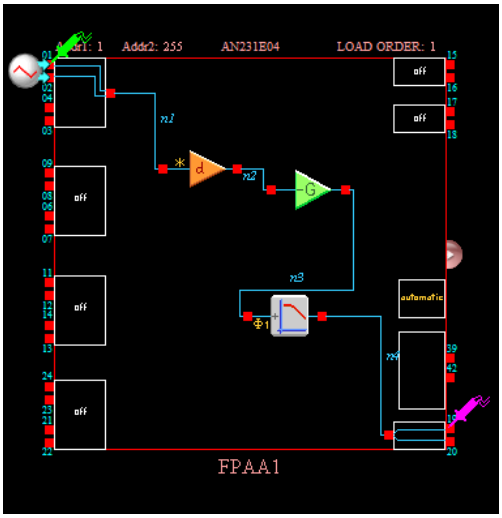


Figure 4.16 Differential block for output response validation.

The differential block setting parameters are the following ones:

- Differentiator CAM clock of 20 kHz
- Input triangle wave, 50 Hz, Vpp = 500 mV.
- Inverted differentiator with differential constant, 2 ms.
- Inverted gain stage with gain = 1.
- Output connected to oscilloscope with 10 ms / 500 mV per division.

Figure 4.17 shows the response of differential block on simulator.

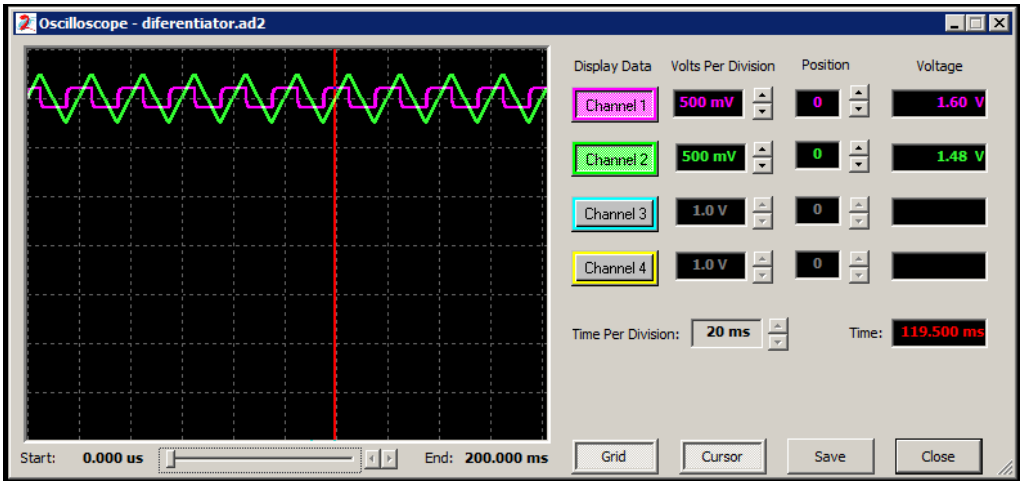


Figure 4.17 Differential block output response with triangle wave input on simulator.

Figure 4.18 shows the response of differential block on oscilloscope.

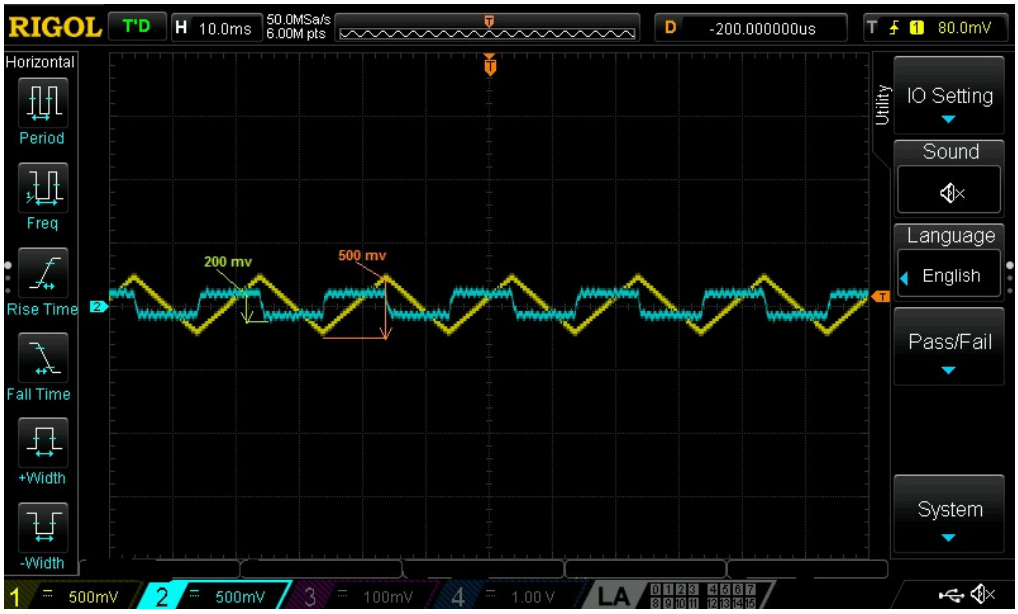


Figure 4.18 Differential block output response with triangle wave input on osciloscope.

The obtained noise on output makes necessary to include a low-pass bilinear filter following the differential plus gain stage CAMs on block design to reduce the noise. After making trials with several corner frequencies f_0 and checking with oscilloscope, the best compromise was to set f_0= 500 Hz. Despite of noise, the results on simulator compared with measured wave forms on oscilloscope are very similar in terms of signal amplitudes and expected wave shapes.

Considering the addition of a bilinear filter as mention before, the complete circuit of differential block diagram with low pass filter and corner frequency f_0 is shown in Figure 4.19.

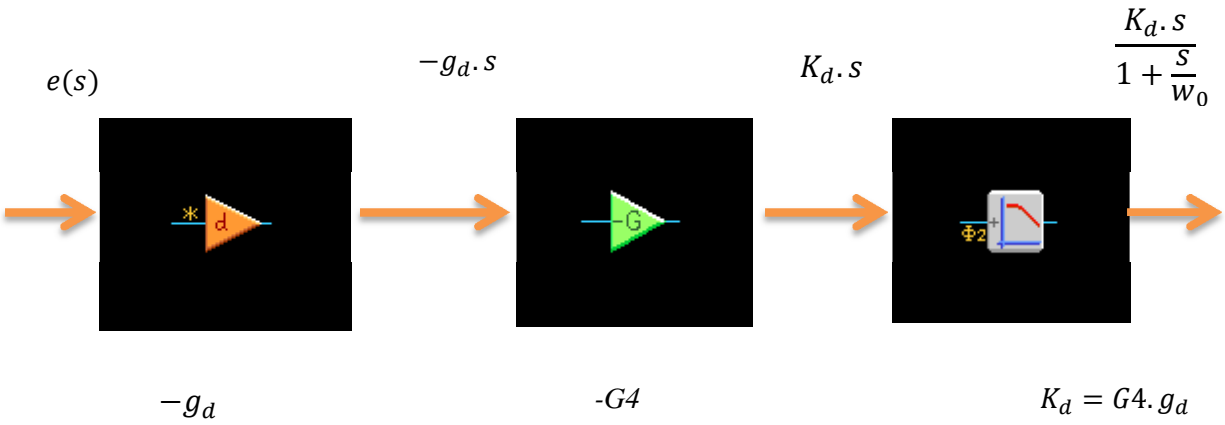


Figure 4.19 CAM design for complete differential control block diagram with low pass filter.

Next block circuit has the function to sum proportional, integral and differential effects for the PID controller action. The block is an half cycle sum/difference stage CAM followed by a unit gain bilinear filter CAM that has the main function of mitigate the noise generated by the sum/difference CAM. Figure 4.20 shows the circuit diagram.

It was added a DC voltage CAM on input channel of half cycle sum CAM to program, if necessary, an additional offset DC value.

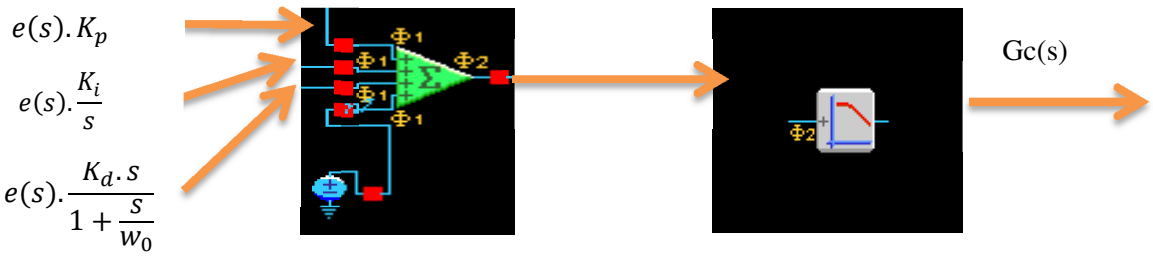


Figure 4.20 CAM design for sum the P, I and D control effects and noise filtering implementation.

The PID circuit is implemented on two dpASPs/FPAAs due to limited resources of a single device to accommodate the described circuit design as shows Figure 4.21.

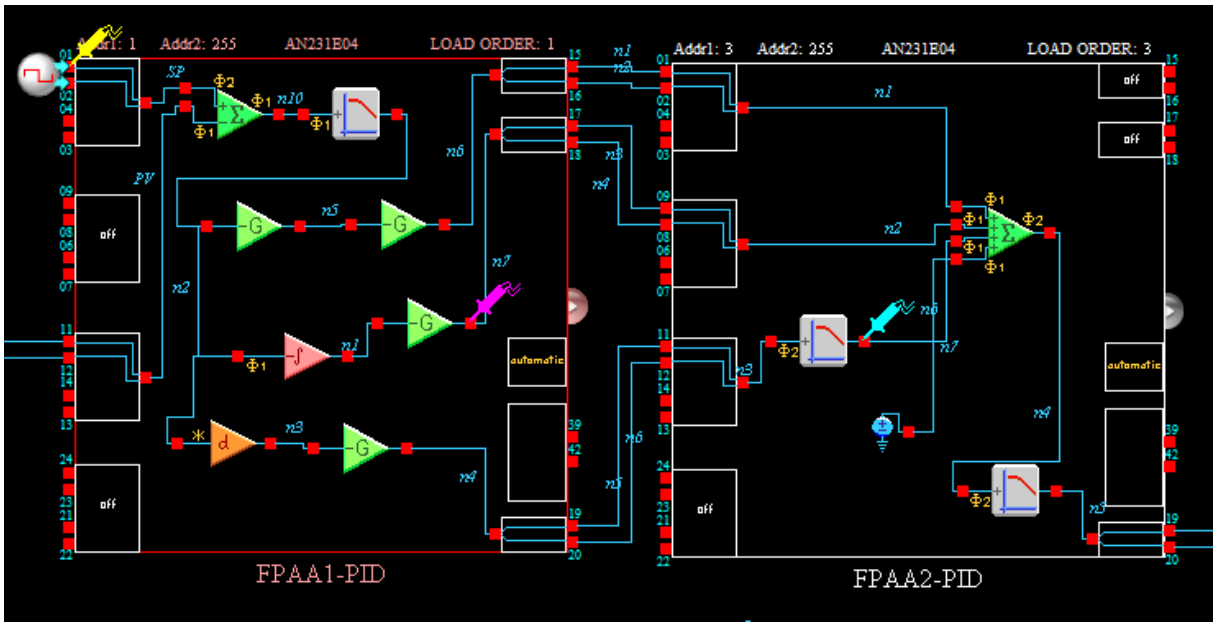


Figure 4.21 PID controller implementation using two FPAA/dpASPs AN231E04.

Several applications require different ranges to select K_p, K_i and K_d parameters. However the differential time constant from differential CAM and integration time constant from integration CAM is limited to a range automatically selected by AnadigmDesigner 2 based on chosen system clock. Then, the implementation of gain stages on PID design with two FPAA devices as shown on Figure 4.21, gives more flexible on the available settings for the PID gain parameters K_p, K_i and K_d.

To evaluate the performance of PID controller design on AN231E04 dpASP/FPAAs, it is compared the system step response on AnadigmDesigner2 simulator with the system step response with PID controller modeled with same setting parameters on MATLAB/SIMULINK. The plant used for validation is the same for both cases.

4.3 PID CONTROLLER DESIGN EVALUATION

To perform evaluation of PID design, it is executed the following procedure:

- Model a plant dynamic system by a transfer function of second order on MATLAB and AnadigmDesigner 2. Compare results of open loop step response of transfer function.
- Model a PID controller on MATLAB and AnadigmDesigner2.
- Compare results of closed-loop unit step response for various values of K_p, K_i and K_d.

For evaluation proposes, it was selected a second order plant. The setting parameters of transfer function on AnadimDesigner2 are (G =1, $f_0 = 5$ Hz, $Q = 1$) :

$$\frac{V_{Out}(s)}{V_{In}(s)} = \frac{4\pi^2 \times {f_0}^2 \times G}{s^2 + \frac{2\pi \times f_0}{Q} s + 4\pi^2 \times {f_0}^2} = \frac{{\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2} = \frac{987}{s^2 + 31.42s + 987} \qquad (4.5)$$

This transfer function has conjugated complex poles as follows:

$p1 = -15.71 + 27.21j$
$p2 = -15.71 - 27.21j$

The system is stable, as poles are placed on left half-plane of *s* plan.

The open-loop plant transfer function has the following step response as shows Figure 4.22, using AnadigmDesigner2 simulator and MATLAB.

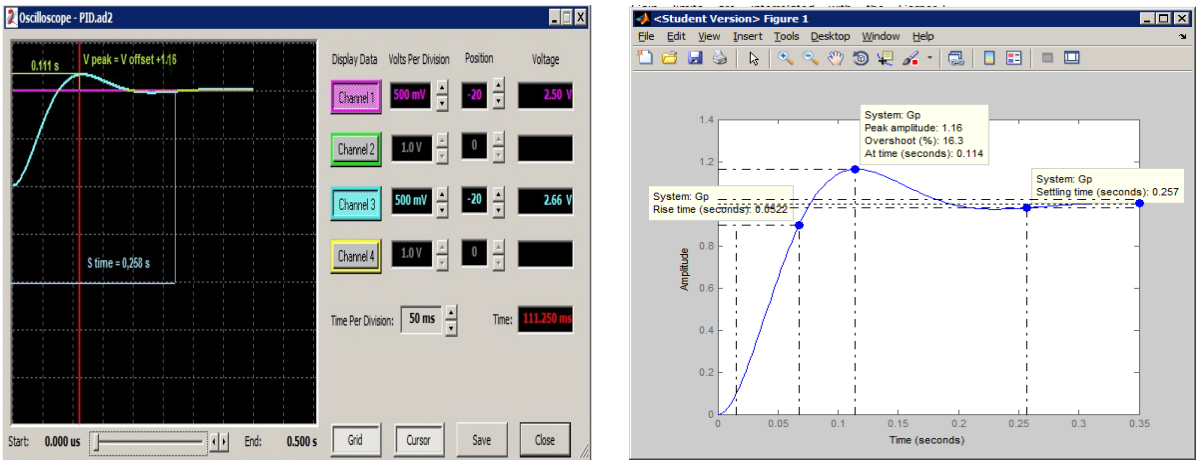


Figure 4.22 Open-loop step response of second order plant system.

Comparing the results of Figure 4.22, it is possible to validate the plant transfer function model implemented on the FPAA. The overshoot and settling time have very similar values on both cases.

To evaluate the closed-loop system with PID controller, it is implemented the design according Figure 4.23. FPAA1 and FPAA2 are used for PID controller and FPAA3 is used to simulate the second order plant transfer function.

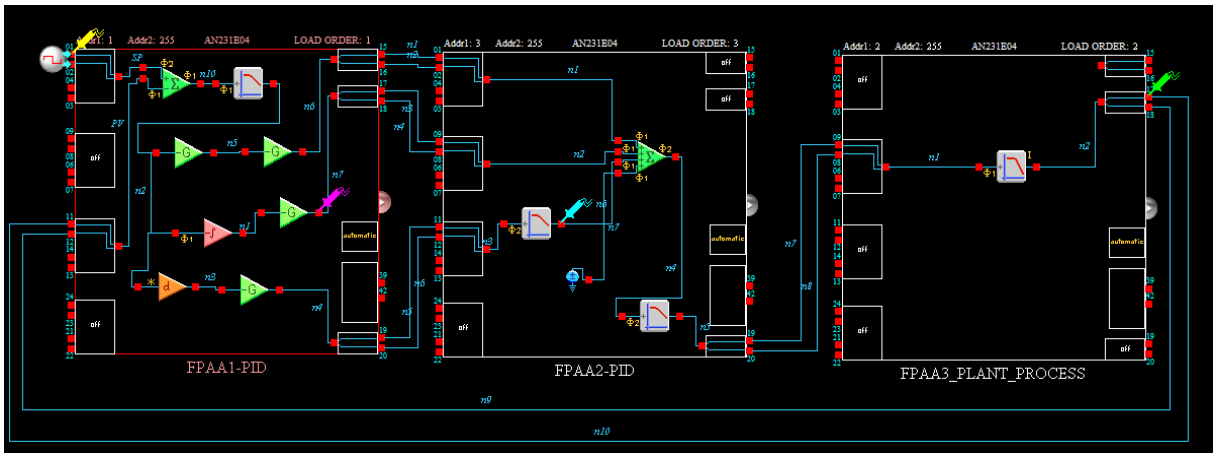


Figure 4.23 Closed-loop PID control system on FPAA/dpASP AN231E04 device.

Figure 4.24 shows the results of step response of closed-loop system using MATLAB and AnadigmDesigner2 simulator for a unit proportional controller ($K_p = 1$).

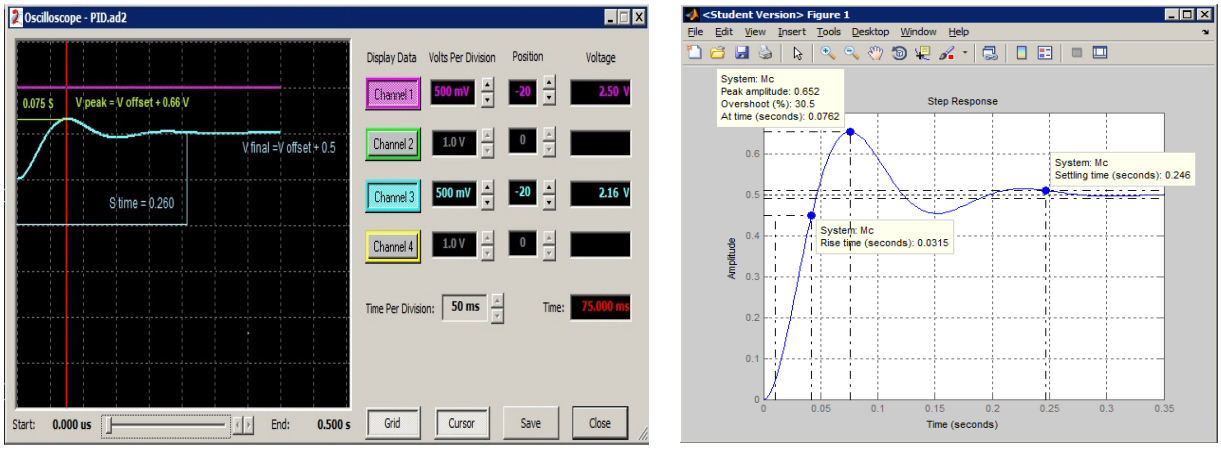


Figure 4.24 Step response of closed-loop system with P controller : $K_p = 1$, $K_i = 0$ and $K_d = 0$.

Comparing the results, it is possible to evaluate the PID design feedback closed-loop system which have very similar values for overshoot and settling time.

Next evaluation of PID design is using PI controller with ($K_p = 5$, K_i =50 and $K_d = 0$). Figure 4.25 shows the results of closed-loop step response with input step value 250 mV to avoid saturation on integrator, using MATLAB and AnadigmDesigner2.

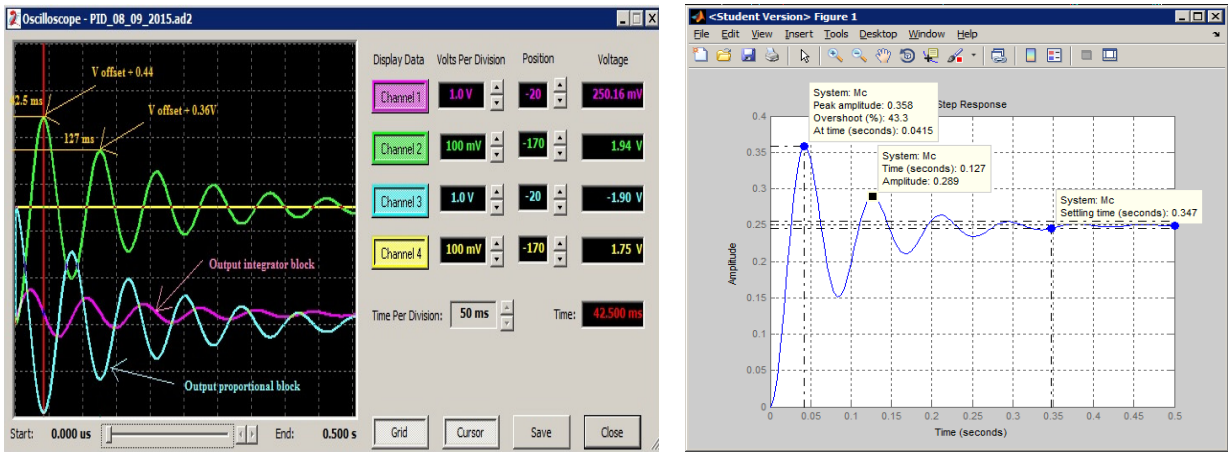


Figure 4.25 Closed-loop step response with PI controller: $K_p = 5$, $K_i = 50$ and $K_d = 0$.

Comparing the results, it is possible to evaluate the PID design feedback closed-loop system; the overshoot and settling time have very similar values.

In the next evaluation of PID design it is included a derivative control block and increased integrator gain ($K_p = 5$, $K_i = 100$ and $K_d = 0.035$), which is expected to reduce overshoot.

Considering these gain parameters, it is possible to obtain the step response of closed-loop PID controlled system.

Using input step value of 250 mV to avoid saturation on integrator, the responses on simulator and MATLAB are shown in Figure 4.26.

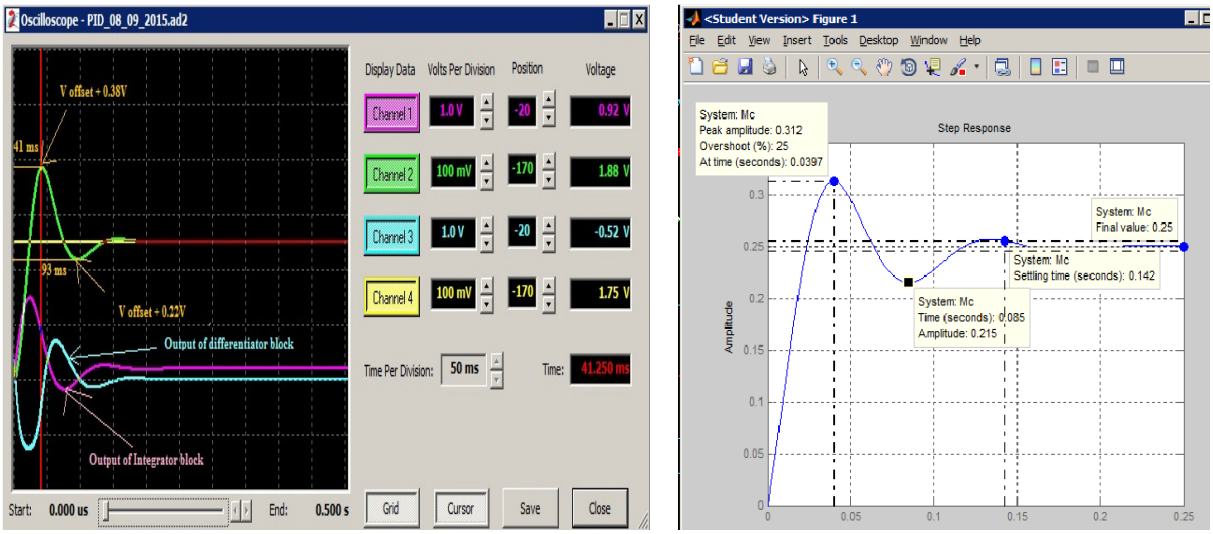


Figure 4.26 Step response of closed-loop with PID controller: $K_p = 5, K_i = 100$ and $K_d = 0.035$.

Comparing the results, it is possible to evaluate the PID design feedback closed-loop system, in which the overshoot and settling time have very similar values and reduced overshoot by inclusion of derivative control.

4.4 FPPA APPLICATION OF ZIEGLER-NICHOLS METHODS

To perform evaluation of the two methods of Ziegler Nichols applied to FPAA technology it is implemented a closed-loop control design on three FPAA/dpASPs, as shown in Figure 4.27.

FPAA1_PID and FPAA2_PID are used for PID controller and the third FPAA_PROCESS is used to simulate a first order plant with time delay.

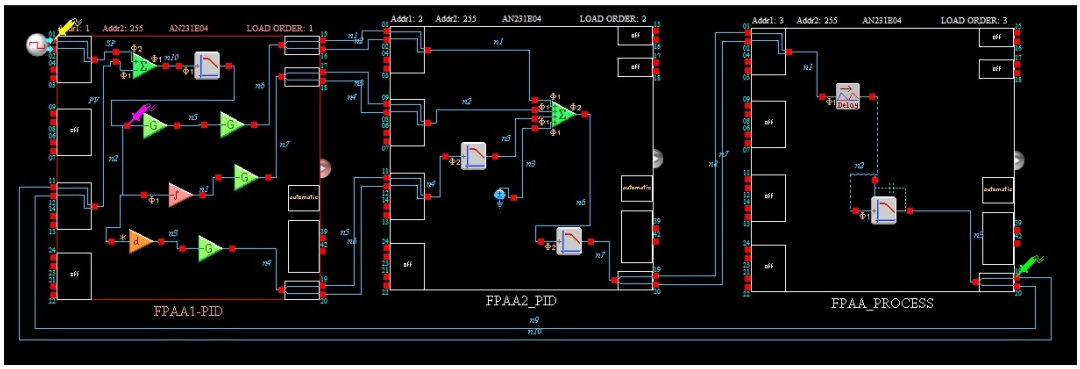


Figure 4.27 Closed-loop PID controller and first order plant process with time delay.

This design will be the basis for the evaluation of the first method and second method of Ziegler Nichols.

4.4.1 APPLICATION OF OPEN LOOP STEP RESPONSE WITH FIRST METHOD OF ZIGLER-NICHOLS

For the first method of Ziegler Nichols, the third FPAA simulates the plant, as illustrated in Figure 4.28, as illustrative example.

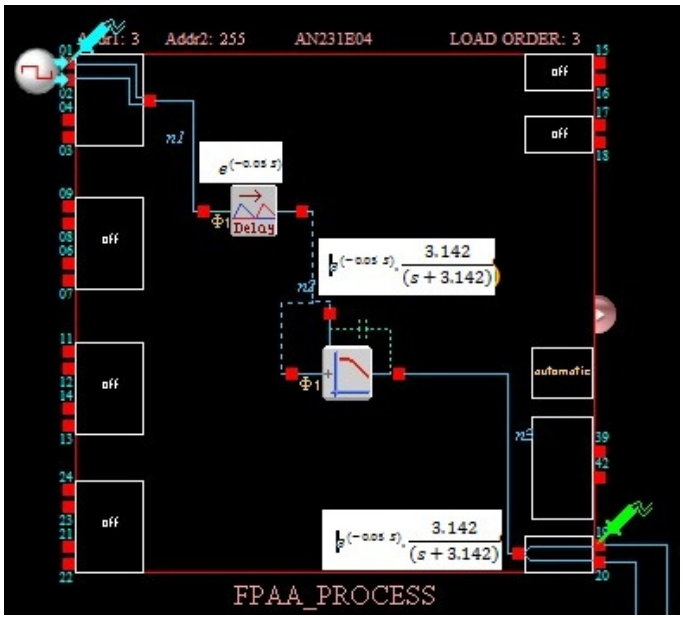


Figure 4.28 Detail of plant model implemented on third FPAA.

Then it is obtained the step response of transfer function as shows Figure 4.29.

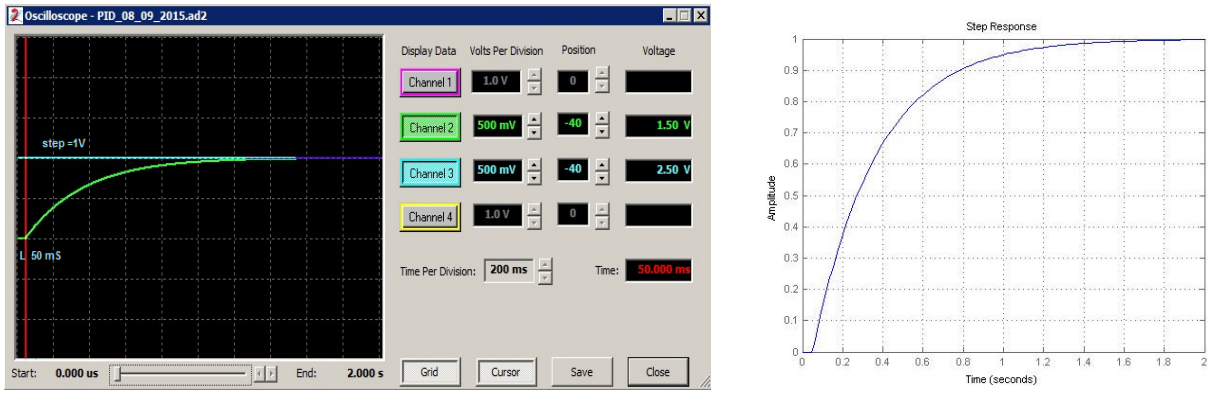


Figure 4.29 Step response of open-loop plant on simulator (left) and MATLAB (right).

The next step is to calculate the parameters τ , R and A according the method described on chapter 4.1.1. (Figure 4.30).

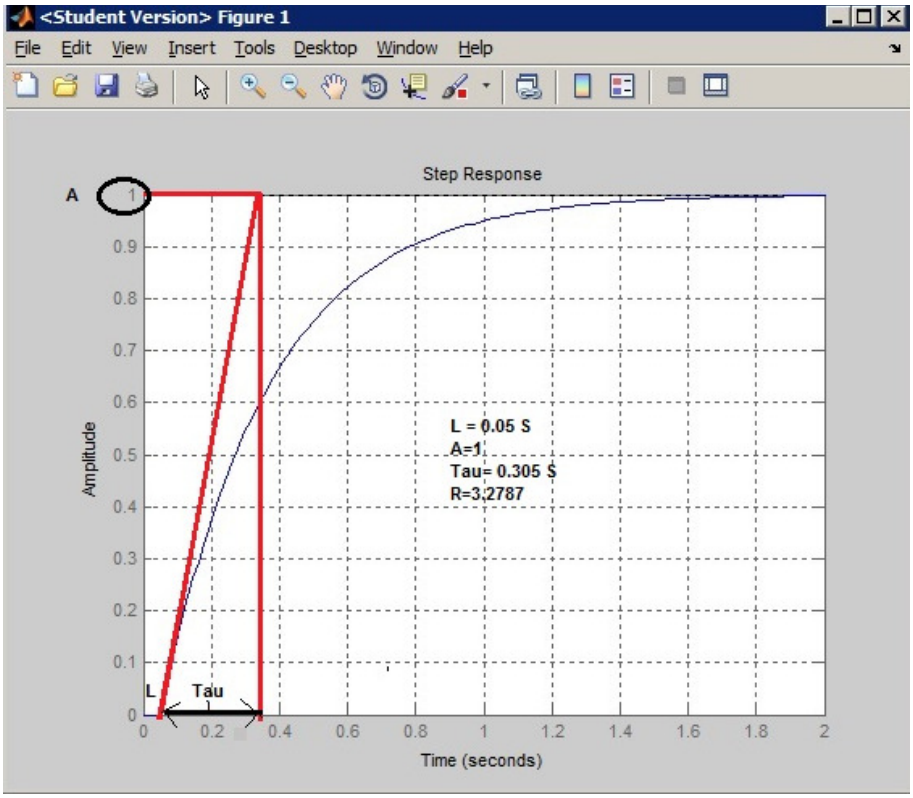


Figure 4.30 Diagram to calculate the parameters of plant model.

The setting PID parameters are (see Table 4.1):

- K_p=6.1
- T_i=0.1 => K_i=61
- T_d=0.025 => K_d=0.153

Figure 4.31 shows the step response with implemented parameters. Green color curve is the response from the plant and blue color curve is the error input for the PID controller. It is applied a step function of 100 mV to the reference input, represented in yellow color.

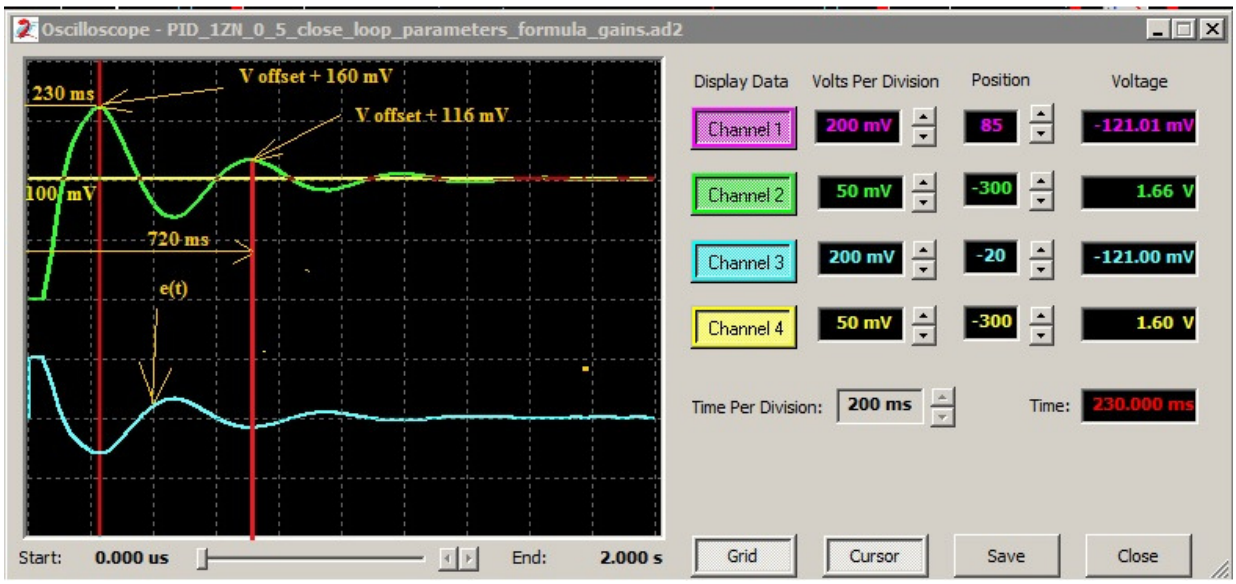


Figure 4.31 Closed-loop step response with PID parameters according first method of Ziegler-Nichols.

As it can be seen on previous figure, the decay of oscillation is near a quarter amplitude which is according the Zigler-Nichols criteria. As already shown on Figure 4.5, the controller parameters are designed to result in a closed-loop step response transient with a decay ratio of approximately 0.25. This means that the transient decays to a quarter of its value after one period of oscillation.

4.4.2 APPLICATION OF CLOSED-LOOP CRITICAL GAIN WITH SECOND METHOD OF ZIEGLER-NICHOLS

For the second method of Ziegler-Nichols, it is used the closed-loop design as shown on Figure 4.27. The PID parameters should be set to K_i =0 and K_d=0. Then, increase parameter K_p step by step until reach the margin of instability. At this point it is obtained the critical gain and the corresponding critical period, as demonstrated in Figure 4.32.

- K_u =10.6
- P_u =0.189 s

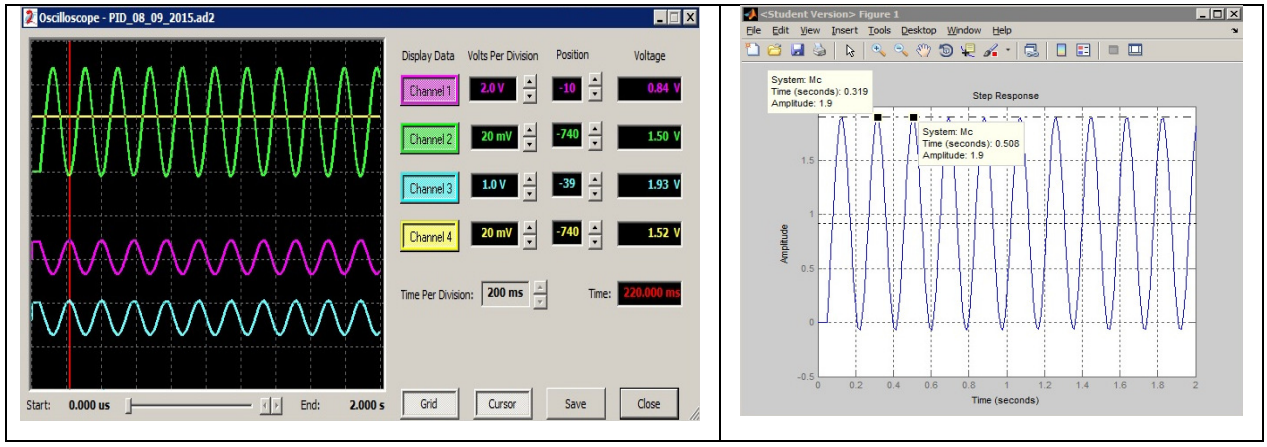


Figure 4.32 Critical gain and period of closed-loop system on simulator (left) and MATLAB (right).

The setting PID parameters are (see Table 4.2):

- K_p=6.36
- T_i=0.095 => K_i = 67.3
- T_d=0.0235=> K_d = 0.15

After setting these parameters on PID controller (FPAA1 and FPAA2) it is possible to obtain the step response of closed-loop system as shows Figure 4.33. Green color curve is the response of the plant model and blue color curve is the error at PID input. It was used a step function of 100 mV of amplitude, represented in yellow color.

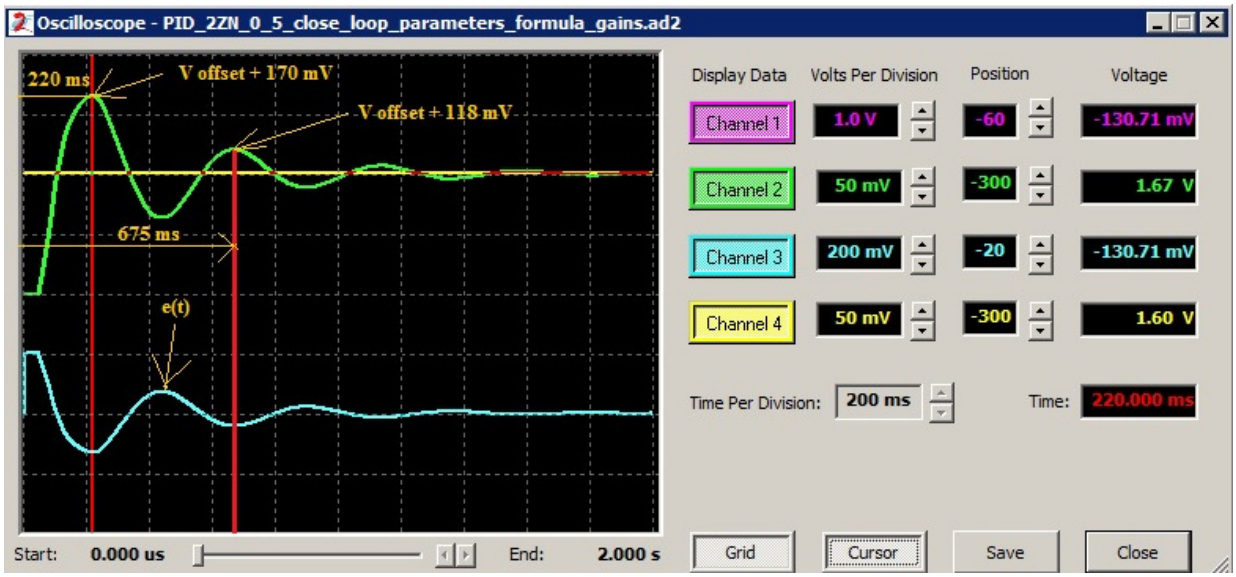


Figure 4.33 Closed-loop step response with PID parameters according second method Ziegler-Nichols.

As it can be seen on previous figure, the decay ratio of oscillation is near a quarter amplitude which is according the Zigler-Nichols criteria.

4.5 DISCUSSION

The FPAA is a nice platform to design and implement singled-loop PID controllers. The design of PID controller can be done at block level, simulate and test each circuit in few minutes without the need to do complex mathematical calculations, choosing discrete components, or focus on analog circuit details. However cautions in terms of filtering should be considered during design, especially due to noise on output of differentiator block and also on sum/difference output CAMs. Also, it should be monitored the output of proportional and integrator block using probes during simulation as saturation can occur easily after increase of K_p or K_i. The small DC voltage that was connected to input 4 of half sum/difference CAM has the function to sum the proportional, integral and differential actions. This small DC voltage could be programmed with help of multiplier factor of the input 4 of the sum/dif CAM to obtain very small DC values that in some circumstances improves the response of controller.

Normal device tolerances are within 1%, and the circuit parameter values are immune to changes due to aging and temperature that occur with most analog circuits. Individual parameters, such as gain, can be updated in a few microseconds due to re-configurability on the

fly of dpASPs. The obtained results on AnadigmDesigner simulator are similar to those of MATLAB.

Finally, it is described an example of tuning of PID controller using the methods of Ziegler-Nichols applied to control a first-order plant with time delay. The obtained step responses using both methods shows the quarter decay amplitude between the first and second oscillation which is in accordance on both methods. It is necessary to use a small amplitude step input of 100 mV to avoid saturation of proportional block, especially in the second method when determining the critical gain and period of oscillation. As well the integration block easily saturates which means that should be take always into consideration the evaluation with simulator to check saturation of P, I and D blocks before download the new setting parameters to FPAAs.

On third generation Anadigm dpASP/FPAA, the saturation is internally achieved at amplitude of approximately 3 V and should be considered that VMR level or internal ground signal reference is 1.5 V. These reference voltage levels should be considered during simulation to avoid response errors during implementation of PID controller.

5 FPAA PRACTICAL CONTROL PROJECT

The previous chapter described the design concept and tuning methods of PID controlled systems and implementation on FPAA/dpASP hardware technology. It was described the implementation of PID controller on Anadigm third generation FPAA/dpASP using CAMs library of AnadigmDesigner2 and several technics to avoid noise propagation on the circuit.

This chapter describes a practical control implementation of a PID controller on FPAA/dpASP applied to control the temperature of a closed chamber. The electronic hardware is designed to measure the temperature inside chamber and control and drive the cooling process using an air to air Peltier Thermoelectric assembly and the heating process using two flexible silicone heaters. In addition, to the implementation of PID control, mentioned in Chapter 4, the board from Anadigm with FPAA/dpASP will generate the PWM control signals to the power drivers of thermoelectric assembly module as well to the power drivers of silicone flexible heaters. It is discussed the tuning approach for the system and temperature profiles obtained for a specific setpoint.

5.1 GENERAL DESCRIPTION

Figure 5.1 presents the general block diagram of closed-loop control system implemented on hardware. Setting the reference temperature, the error is the difference between the measured actual value of temperature chamber and the reference temperature. This error is applied to the PID controller which output voltage control signal to the PWM generator. These parts are implemented on three FPAA/dpASPs. The output PWM generator drives the PWM power driver for the heaters or in case of cooling, drives the PWM generator for the Peltier thermoelectric assembly passing in this case through a low pass filter. The chamber temperature is measured by thermocouple type K that is connected to a specialized signal condition board and the voltage signal provided on his output is returned to the PID controller and close the loop. The analog interface for the FPAA/dpASP is made by analog input interface board and output interface board with optical isolation.

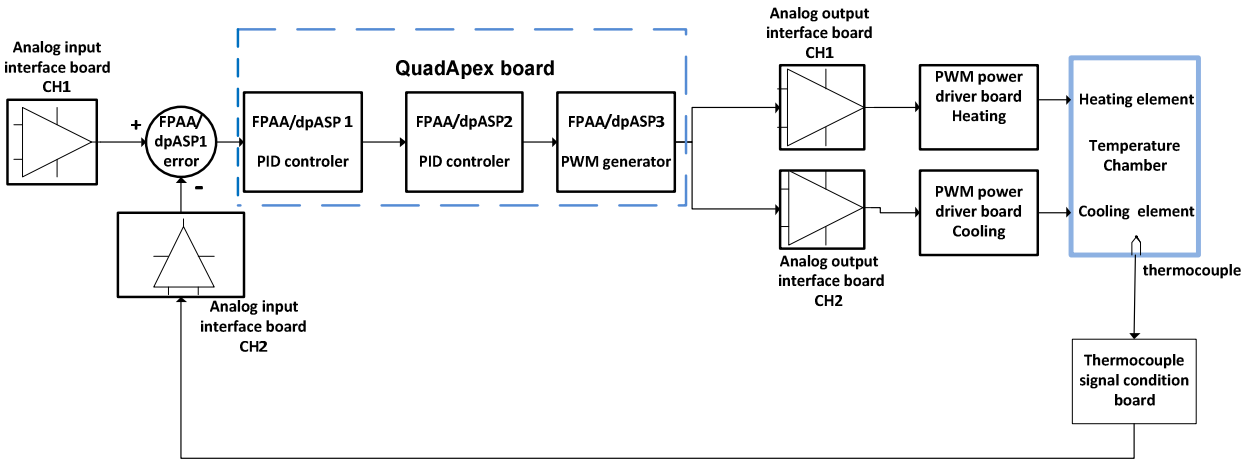


Figure 5.1 General block diagram.

5.2 TEMPERATURE CHAMBER

Temperature chamber is completed closed and thermic isolated, all faces are made in acrylic. Mounted on top, it is installed a thermoelectric assembly element for cooling and on right and left sides are installed silicon flexible heaters for heating. On front side is mounted a thermocouple to measure the actual value of temperature.

5.2.1 HEATING SYSTEM OF TEMPERATURE CHAMBER

Heating system of temperature chamber is performed by two self-adhesive heaters designed for use in areas where standard heating methods are difficult to apply. Silicone rubber heaters with wire-wound elements provide excellent physical strength capable of withstanding repeated flexing without compromising the life and performance of the heater. The wire-wound element process consists of resistance wire wound on a fiberglass cord for added support and flexibility. The wire-wound element is laid out in a special designed pattern to ensure uniform heat profile and to conform to the size and shape of the silicone rubber heater.

The main characteristics of adhesive silicone heater are the following ones:

- Mat Shape : Rectangle
- Peak Temperature : +300°C
- Power Rating : 40 W
- Rectangular Mat Size : 100 x 100 mm
- Supply Voltage : 24 V DC

As already mentioned, the chamber has one flexible heater mounted vertically on the left side and another in mounted also vertically on right side. The total supplied power for the two flexible heaters is 80 W.

Figure 5.2 shows the two adhesive silicon heaters.

Figure 5.2 Silicone flexible heaters [43].

The low thermal mass of flexible heaters allows their use in applications where the space for placing a heater is limited and weight is a concern. They are of low mass construction and provide rapid heat-up, desired requirement for applications where precise temperature control is important to the overall quality of the application. Flexible Heaters are not affected by

mechanical shock, vibration or repeated flexing and will not stretch or tear over a temperature range of -56.6 ºC to +260 ºC.

Typical applications are the following ones:

- Aerospace
- Aircraft Comfort Heaters
- Automotive
- Battery Heaters
- Food Service Equipment
- Incubators
- Laboratory Equipment
- Liquid Reservoirs
- Medical Equipment
- Mirror Heaters
- Optical Equipment
- Outdoor Antennas
- Packaging Machinery
- Semiconductor Equipment
- Vending Machines

5.2.2 COOLING SYSTEM OF TEMPERATURE CHAMBER

The cooling system is implemented using a thermoelectric cooler (TEC), sometimes called as thermoelectric module or Peltier cooler mounted on top of the temperature chamber. This module is made of semiconductor-based electronic components that functions as a small heat pump. By applying a low voltage DC power source to a TEC module, heat will be moved through the module from one side to the other. One module face, therefore, will be cooled while the opposite face simultaneously is heated. It is important to note that this phenomenon may be reversed when changed polarity (plus and minus) applied DC voltage. On this application it is used only for cooling as the mechanical and thermoelectric designed is made for that propose. Figure 5.3 shows a Peltier module with heat and cold side.

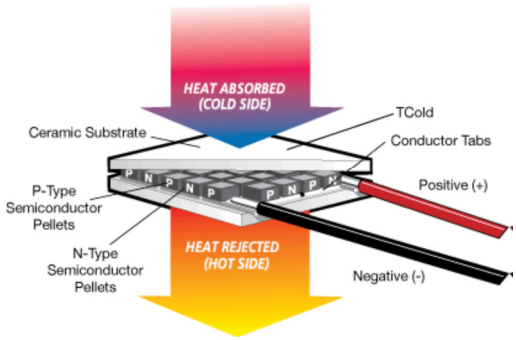


Figure 5.3 Thermoelectric Peltier module [41].

A detailed description of physical principles, advantages and disadvantages and applications can be found on appendix E.

For this application, it was selected an Air-to-Air Peltier thermoelectric assembly (TEA), with reference AA-040-24-22, from Laird Technologies that uses impingement flow to transfer heat. It offers dependable, compact performance by cooling objects via convection. Heat is absorbed and dissipated through high density heat exchangers equipped with air ducted shrouds and brand name fans. The thermoelectric modules are custom designed to achieve a high coefficient of performance (COP) to minimize power consumption. This thermoelectric assembly has right dimensions to fit on the top temperature chamber and power to cool down the air inside it. The thermoelectric assembly has the following main specifications:

- Cooling Power Qcmax : 41 W
- Running Current : 2.6 A
- Startup Current : 3.0 A
- Nominal Voltage : 24 V
- Max Voltage : 30 V
- Power Input : 62 W
- Operating Temperature : -10 to 52 °C
- Weight : 1.8 Kg
- Performance Tolerance : ±10%

Figure 5.4 shows the Peltier thermoelectric assembly from the company Laird Technologies.

Figure 5.4 Peltier air-to-air thermoelectric assembly [44].

5.3 CONTROL SYSTEM

Designing a temperature controlled environment chamber requires taking in consideration different subsystems or functional blocks. In particular, such a device requires a mechanism to modify and change the chamber temperature as desired. In order to control the temperature with accuracy, it is necessary to tune the controller. This chapter discusses the controller block implementation and also subsystems as temperature sensing block, thermoelectric assembly driver circuit and heater driver circuit. The closed-loop control system diagram was shown on previous Figure 5.1.

5.3.1 TEMPERATURE SENSING BLOCK AND SETPOINT SETUP

A thermocouple is positioned inside temperature chamber to measure temperature. This thermocouple is connected to a analog output K-Type Thermocouple Amplifier board that uses IC AD8495. It makes signal conditioning of the signal from thermocouple. The output analog voltage from the four thermocouple amplifier is connected to the second input channel of the input interface board. The output from input interface board is a differential signal with appropriated amplitude to connect to input channel of dpASP/FPAA.

Thermocouples are very sensitive, requiring a good amplifier with a cold-compensation reference. The AD8495 K-type thermocouple amplifier from Analog Devices included on the board should be powered with 3 V to 18 V DC. Measuring the output voltage on the OUT pin, it can be easily converted to temperature with the following equation:

$$Temperature(ºC) = \frac{(Vout - 1.25)}{0.005} \tag{5.1}$$

The corresponding linear transfer function between board output voltages versus measured temperature is shown on Figure 5.5a.

However, the thermocouple board output voltage signal is half attenuated on input interface board to avoid saturation on highest temperatures and added VMR. Figure 5.5b shows the real transfer function considering already the described attenuation and VMR included.

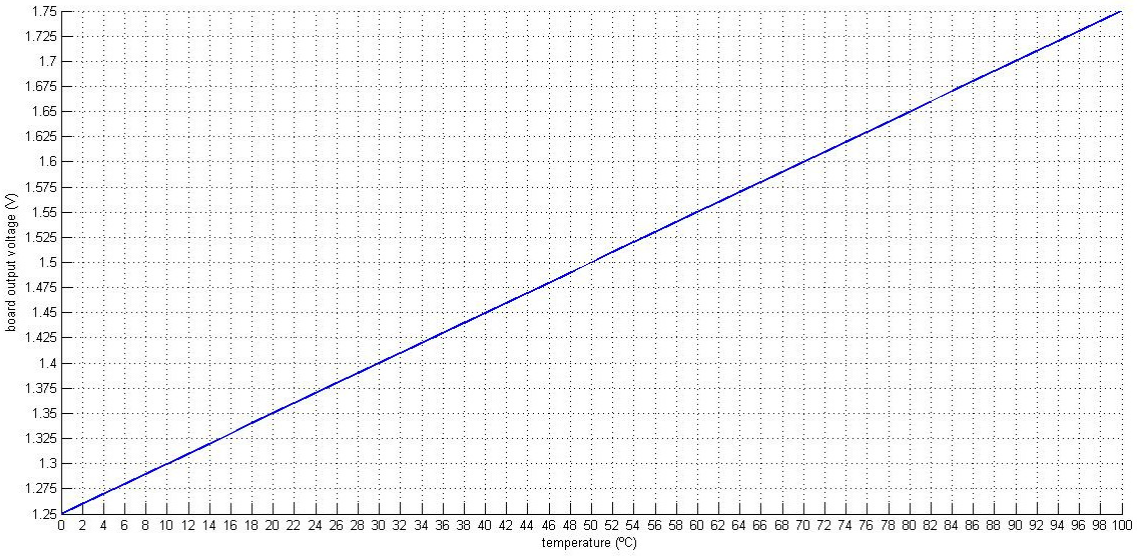


Figure 5.5a Linear transfer function between measured temperature versus board voltage output.

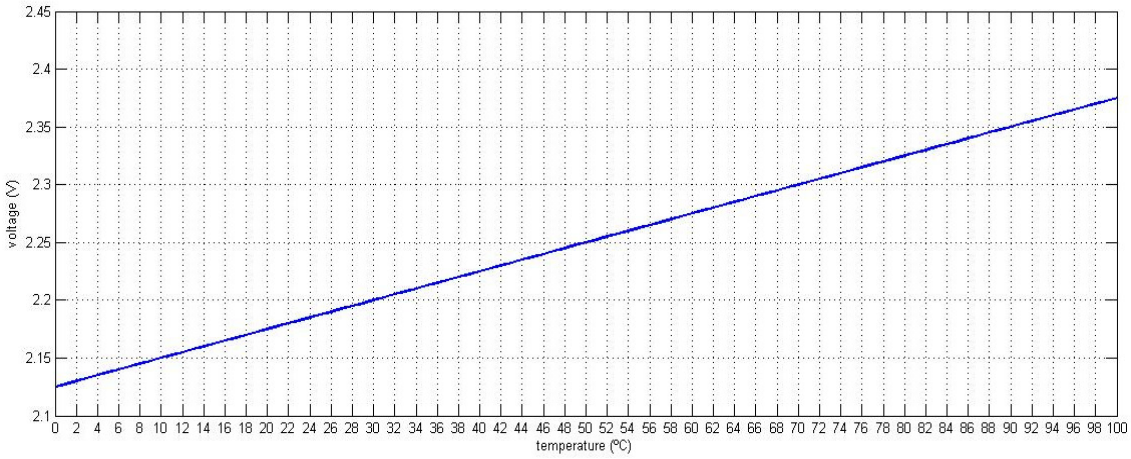


Figure 5.5b Linear transfer function between measured temperature versus input voltage to FPAA.

The board has two pin terminal block for connecting to the thermocouple and is fully assembled on PCB with the AD8495 + TLVH431 1.25 V precision voltage reference and output pin header. With this board should be used only K thermocouple type (Figure 5.6).

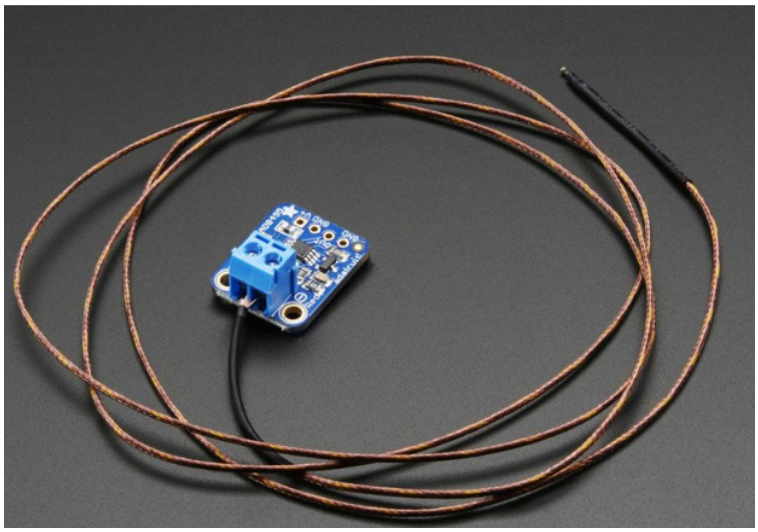


Figure 5.6 Analog Output K-Type Thermocouple Amplifier board with thermocouple [40].

This board from Adafruit company has the following main characteristics:

- Sensing Accuracy Range: ± 1 ºC around room temperature, ± 2 ºC for −25 ºC to +400 °C
- Sensing Temperature Max: 400 ºC
- Sensing Temperature Min: -25 ºC
- Supply Voltage: 3-18 V DC

The desired reference temperature is selected on precision potentiometer connected to channel two of analog input interface board. The output from channel two is connected to input channel of FPAA/dpASP. Figure 5.7 shows the temperature sensing block and setpoint diagram. For larger temperature chambers where it is necessary to monitor temperature in several points inside chamber, it is possible to include more thermocouples and correspondent amplifiers in the circuit according diagram presented on Appendix F.

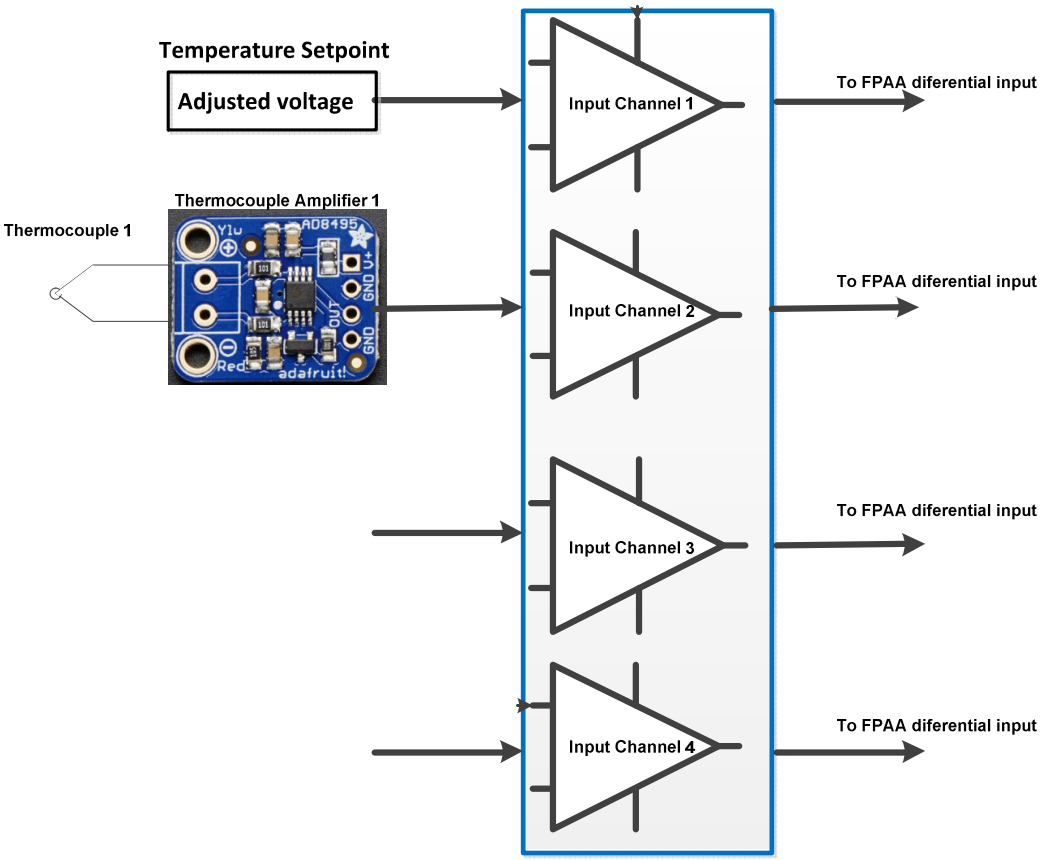


Figure 5.7 Temperature sensing diagram block.

5.3.2 THERMOELECTRIC ASSEMBLY POWER DRIVER CIRCUIT

Thermoelectric assembly is controlled by PID implemented on second dpASP/FPAA. The PID controller output is connected to the third dpASP/FPAA where is generated PWM signal with duty cycle changing proportional to the output voltage from PID controller. Then PWM signal is applied to the input of a power driver circuit. Figure 5.8 shows the picture board from POLOLU - HP Motor Driver (18v15) 15 A, used for Peltier power driver. Normally this board is used for driving large DC brushed motors. However, it can be used to drive other kind of loads as in this case, the Peltier element.

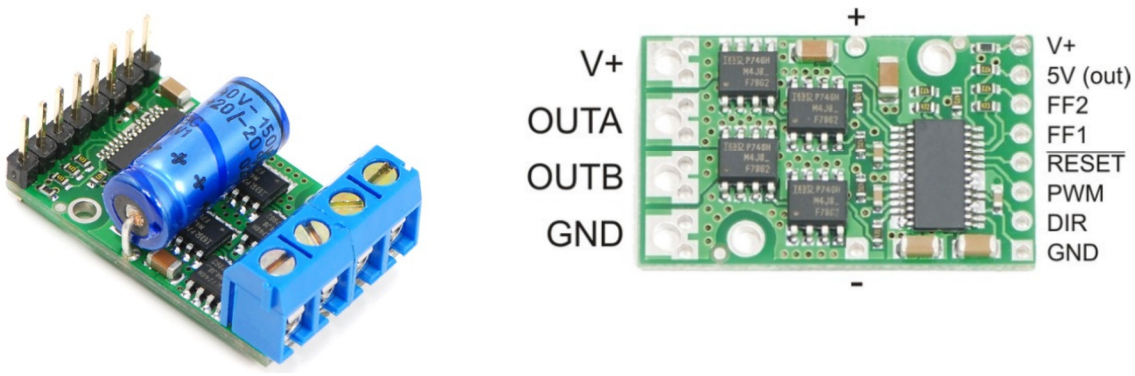


Figure 5.8 PWM power driver board [39].

This board can deliver up to 15 A of continuous current without heat sink. The motor driver supports PWM frequencies as high as 40 kHz, higher frequencies result in higher switching losses in the power driver. The driver can detect three different fault states, which are reported on the FF1 and FF2 pins. The detectable faults are short circuits on the output, under-voltage, and over-temperature. The output from power driver OUT A and OUT B passes by a power filter. Figure 5.9 shows a schematic of the power filter and Peltier assembly load. The LC filter converts the square wave power signal coming from the PWM driver into a low ripple DC (zero frequency) signal. As the square wave is composed of an infinite sum of harmonics, then implementation of LC filters remove all the harmonics except the DC component, and the amplitude of the DC component is directly proportional to the duty cycle of the PWM signal. These filters are required, because the thermal stress generated in the Peltier material when applying fast transients can shorten its life. The manufacture recommends that Peltier element should not have more than 10% ripple.

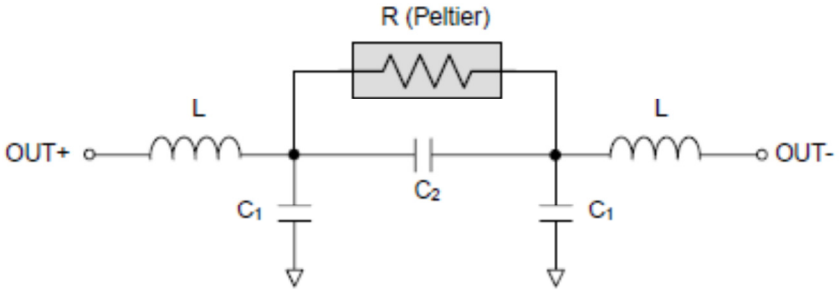


Figure 5.9 Schematic of LC filter [45].

The transfer function for this LC filter is:

$$\frac{V_r(s)}{V_i(s)} = \frac{1}{L(C_1 + 2C_2)s^2 + \frac{2L}{R}s + 1} \tag{5.2}$$

Previous equation (5.2) can be rearranged into standard form for a second-order linear time-invariant system as follows:

$$\frac{V_r(s)}{V_i(s)} = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

$$\omega_n^2 = \frac{1}{LC_1 + 2LC_2} \tag{5.3}$$

$$\xi = \frac{1}{R}\sqrt{\frac{L}{C_1 + 2C_2}}$$

The chosen values for the components are:

- L_1 = 1 mH
- L_2 = 1 mH
- C_1 = 5 µF
- C_2 = 5 µF
- C_3 = 5 µF

The calculated corner frequency and damping ratio values are:

$$\omega_n = 8165 \text{ rad/s}$$

$$f_n = 1300 \text{ Hz}$$

$$\xi = 0.887$$

Figure 5.10 shows the LC filter model on power electronics simulator PSIM.

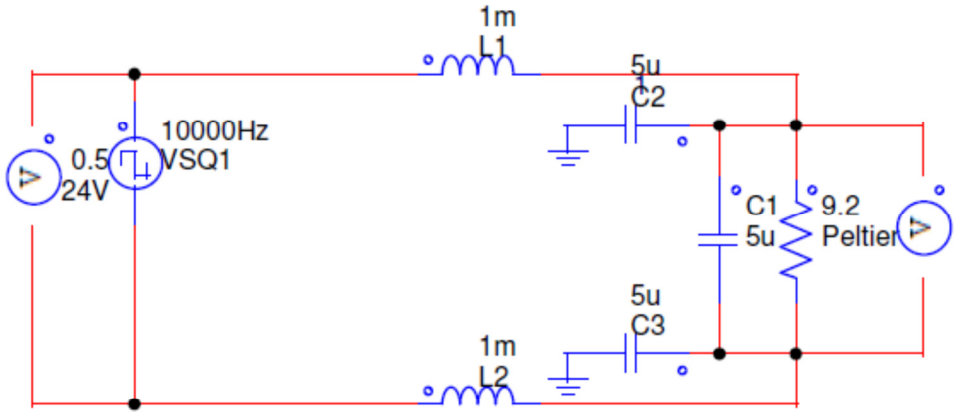


Figure 5.10 PWM LC filter circuit model on PSIM.

It is evaluated output response of the LC filter with duty cycle of 50%, when occurs worst case scenario of output ripple. Then make evaluation of output response with 100% duty cycle without overshoot which should always be avoided to preserve life time TEC module and finally the response with duty cycle of 10% which confirms the small output ripple below 10%.

The achieved voltage output values for the three cases permit to say that there are a linear correlation between duty cycle of input PWM duty cycle signal and DC output from LC filter as it is mandatory. The linear correlation is valid if compared DC output values when steady state regime is achieved.

Figures 5.11a), 5.11b) and 5.11b) show the responses for the three evaluations done with different duty cycles values.

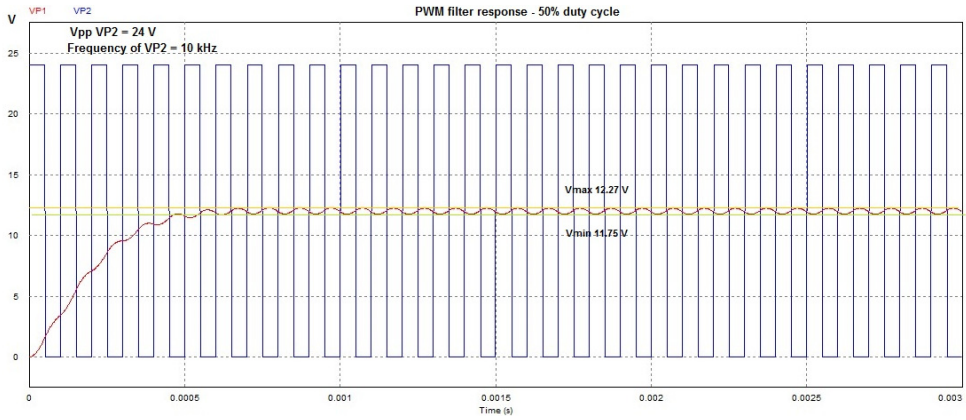


Figure 5.11a) LC filter simulation with duty cycle of 50% using PSIM.

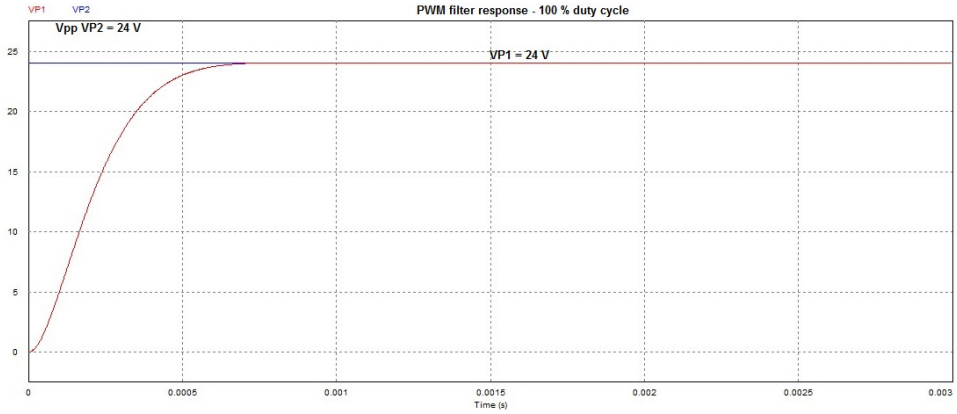


Figure 5.11b) LC filter simulation with duty cycle of 100% using PSIM.

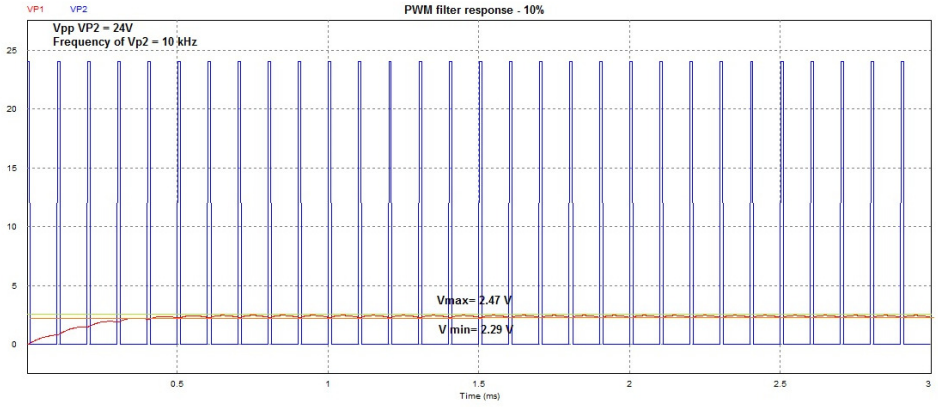


Figure 5.11.c) LC filter simulation with duty cycle of 10% using PSIM.

Figure 5.12 shows the hardware circuit implementation of the LC power filter.

Figure 5.12 LC power filter implementation.

Figure 5.13 shows the complete thermoelectric assembly power driver block diagram considering the calculated values.

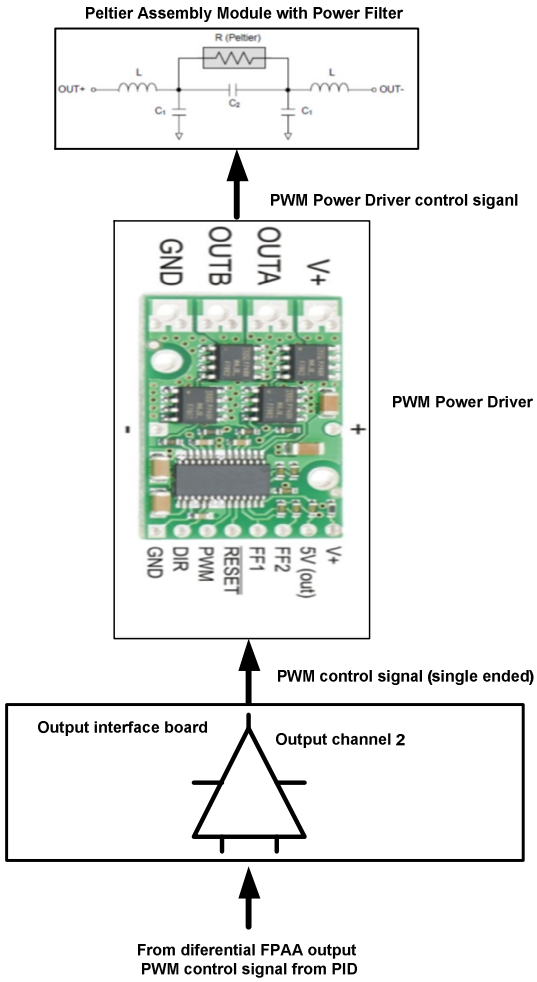


Figure 5.13 Thermoelectric assembly power driver block diagram.

5.3.3 HEATER POWER DRIVER CIRCUIT

Two silicone flexible heaters are connected in parallel and controlled by PID controller implemented on second FPAA/dpASPs. The PID controller output is connected to the third FPAA/dpASPs where is generated PWM signal with duty cycle changing proportional to the output voltage from PID controller. Then PWM signal is applied to the input of a power driver circuit. The POLOLU - HP Motor Driver (18v15) 15 A was used for heater power driver. The PWM signal is applied directly to the heaters. Figure 5.14 shows the block diagram of heater power circuit.

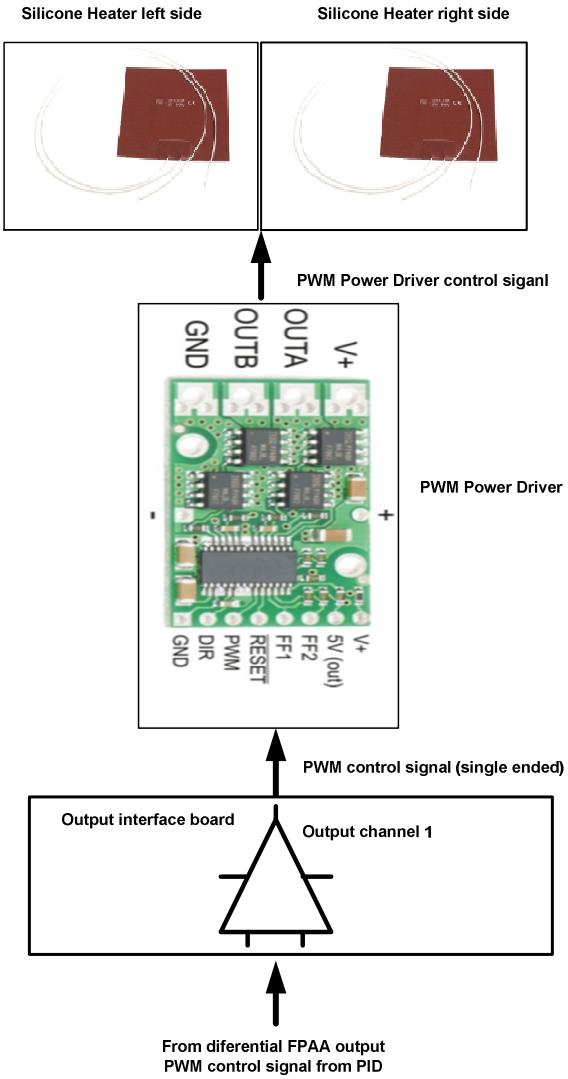


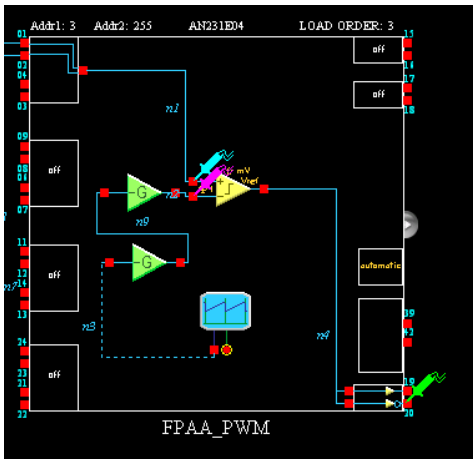
Figure 5.14 Heater power driver block diagram.

5.3.4 FPAA/dpASP CONTROL CIRCUIT

During development of this Thesis, Anadigm released a new board on April, named Anadigm QuadApex which have four FPAA/dpASPs third generation devices. The same device described on chapter 2 and used on board described on chapter 3, the AnadigmApex AN231K04-DVLP3. The chapter 5 uses the new board version, the schematics and picture are shown on Appendix D. The new board has more integration and included microprocessor was upgraded to PIC32. The connections between ports of the FPAA/dpASP devices can be set by micro switches avoiding the installation of twisted pair connection cables. From the four FPAA/dpASPs available on board will be used three of them.

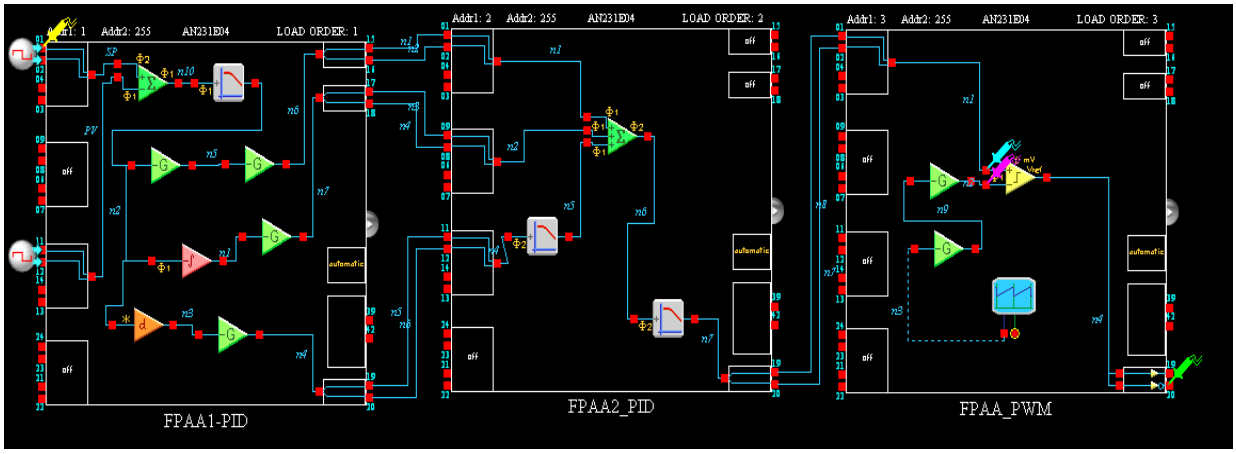
The error correction algorithm adopted for the system is a proportional, integral and derivative (PID) controller. PID control systems are three-term control systems already described on chapter 4 in terms of tuning parameters and implementation on the FPAA/dpASP devices from Anadigm. The PID controller is the main component of the control system block. The temperature is measured inside chamber by thermocouple which gives the feedback PV value. It is implemented a PWM design module on a third FPAA that receives the output signal from PID controller on his input and generates the correspondent PWM signal on his output. Then, PWM generator will send the signal for each PWM power driver board which has a H-bridge power circuit able to provide PWM power signal to the silicon flexible heaters in case of heating process or in case of cooling process give the PWM power signal to the power filter of Peltier thermoelectric assembly module.

The PID design is implemented on two FPAA/dpASPs according description in chapter 4. Regarding PWM generator receives the voltage control signal from PID controller and generates PWM output signal with duty cycle proportional to the input voltage level. Figure 5.15 shows the PWM design implemented on the third FPAA/dpASP.



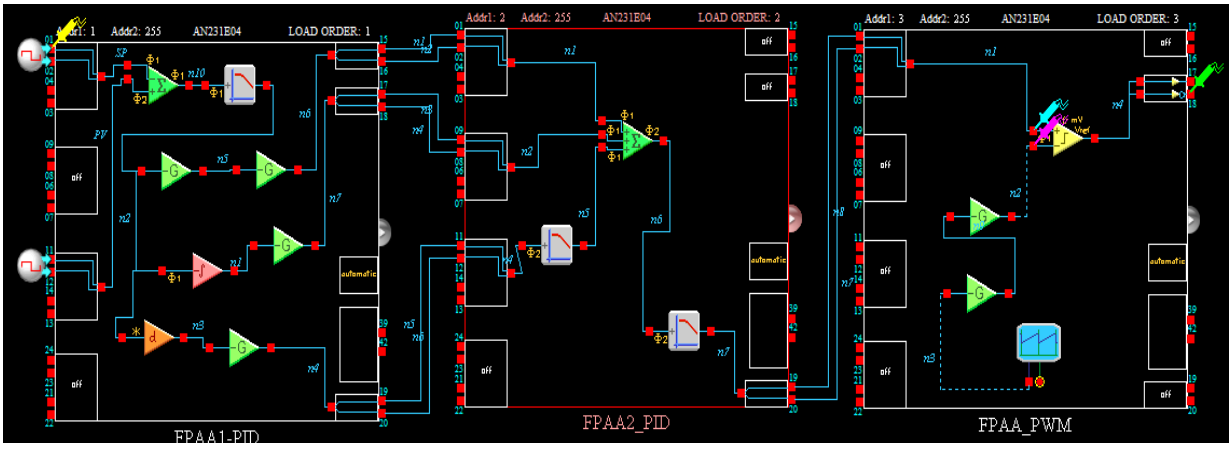
5.15 PWM generator implemented on third FPAA/dpASP.

The complete design of PID and PWM generator implemented on AnadigmQuadApex board for the heating process is shown on Figure 5.16.



5.16 Controller with PWM generator for heating design implemented on QuadApex board.

The complete design of PID and PWM generator implemented on AnadigmQuadApex board for the cooling process is shown on Figure 5.17.



5.17 Controller with PWM generator design for cooling implemented on QuadApex board.

All connections of I/O differential ports between dpASPs are made with two twisted wires.

5.4 TRANSFER FUNCTION OF HEATING AND COOLING PROCESS

It is performed four experiments to obtain the dynamic response of the heating and cooling temperature process.

The equipment used for these experiments where the following ones:

- Two DC power supplies with regulation.
- Multimeter with temperature data-logger and transmission data by USB to monitor PC.
- Thermocouple to connect to multimeter and measure temperature inside the chamber.

The record of temperature is settled on data-logger to make measurements with interval of 15 s. Figure 5.18 shows the setup of the experiment when temperature inside chamber is rising. The transfer function is obtained by PC connected to multimeter data-logger.

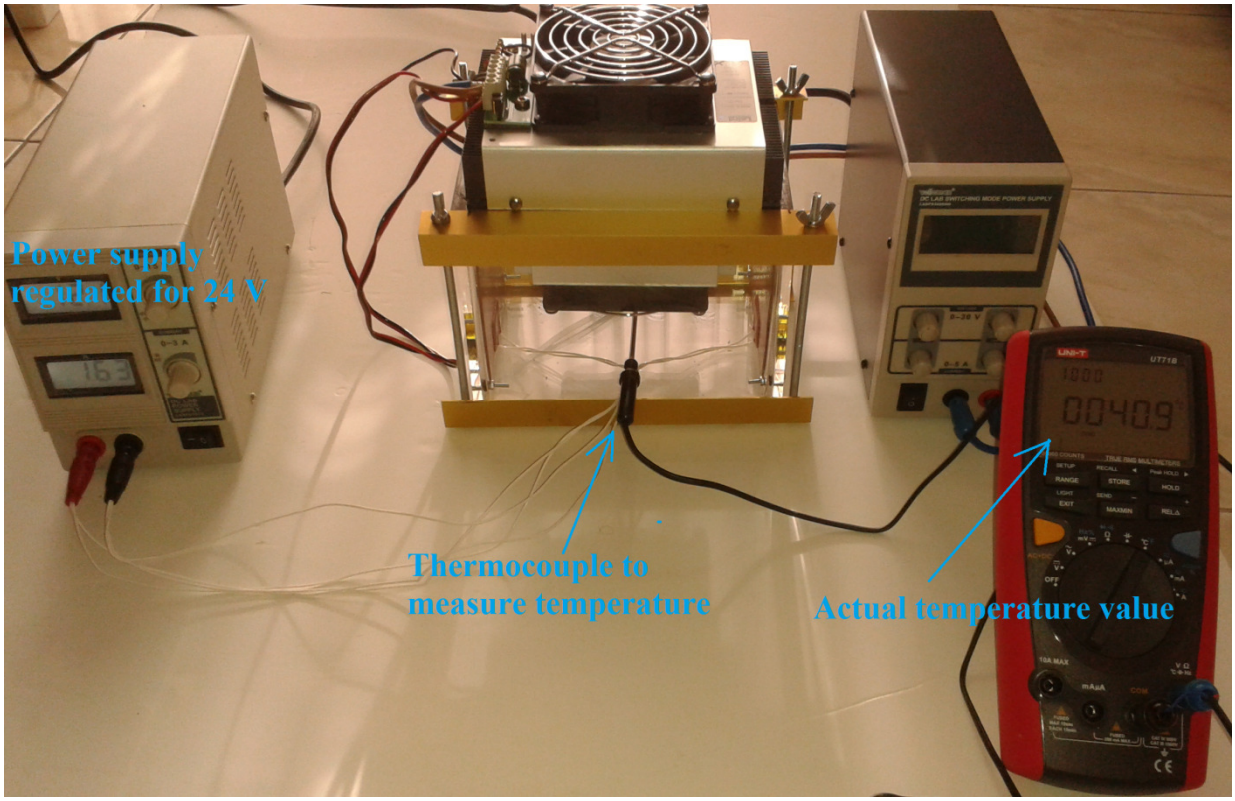


Figure 5.18 Experiment to obtain the response of heating process.

Figure 5.19 shows the setup of the experiment for temperature inside chamber during cooling process. The transfer function is obtained on PC connected to multimeter data-logger.

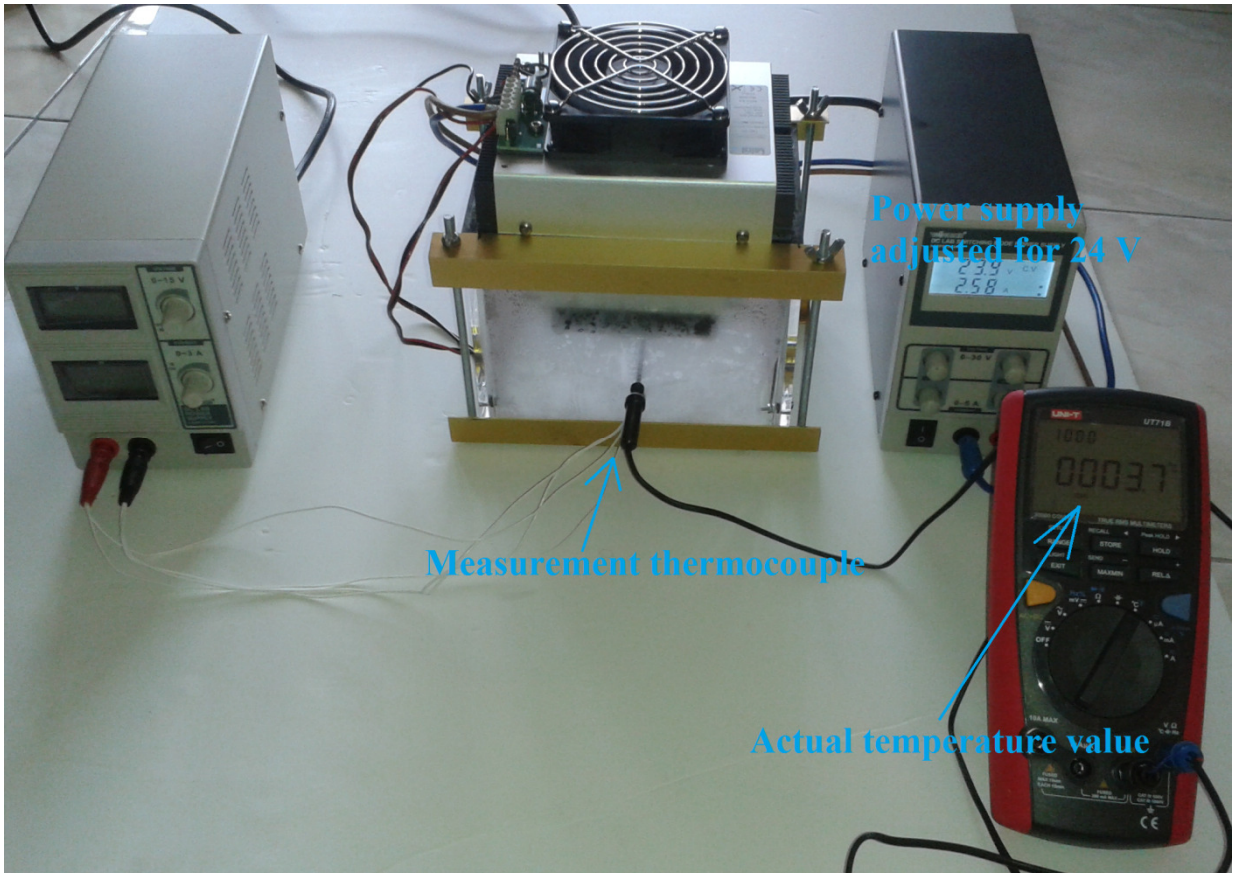


Figure 5.19 Experiment to obtain the response of cooling process.

Figure 5.20 shows the dynamic response during heating from ambient to maximum temperature when is applied 24 V to the heaters. The data was imported to MATLAB to plot the curve.

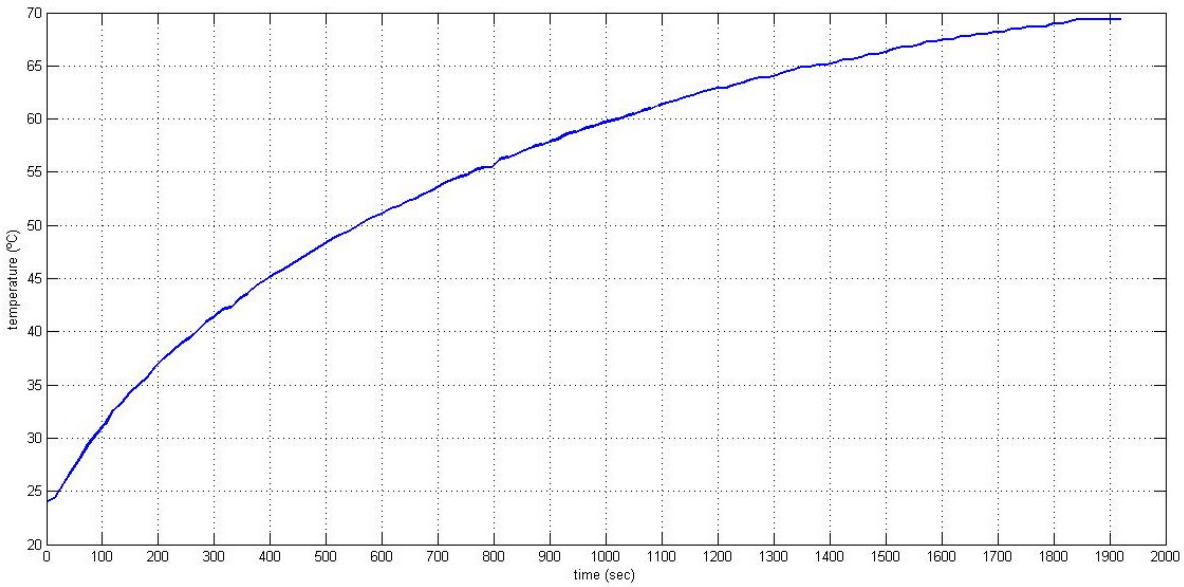


Figure 5.20 Dynamic response of system during heating from ambient to maximum temperature.

Figure 5.21 shows the dynamic response during heating from coldest temperature to maximum temperature when is applied 24 V to the heaters. The data was imported to MATLAB to plot the curve.

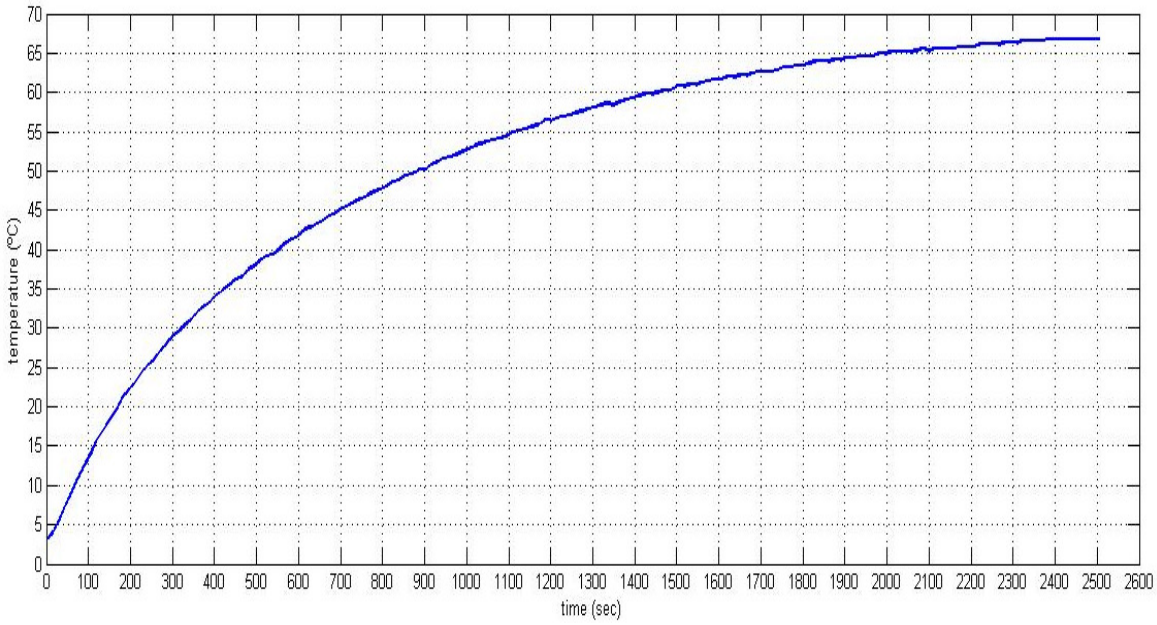


Figure 5.21 Dynamic response of system during heating from coldest to maximum temperature.

Figure 5.22 shows the dynamic response during cooling from ambient temperature to cold temperature when is applied 24 V to the Peltier assembly module. The data was imported to MATLAB to plot the curve.

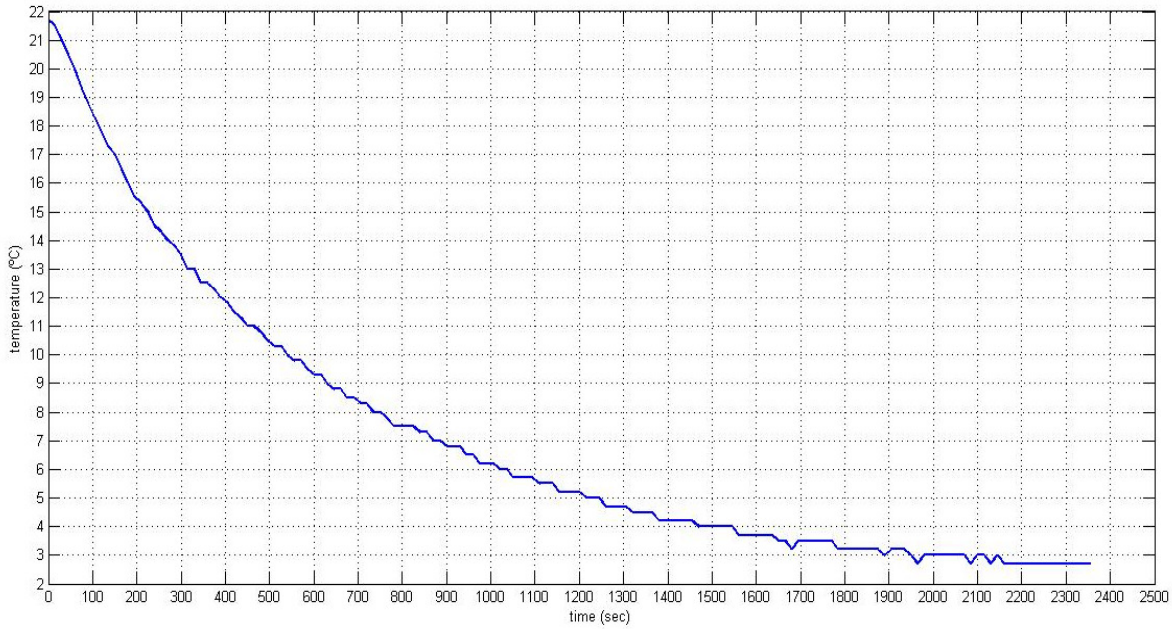


Figure 5.22 Dynamic response of system during cooling from ambient to coldest temperature.

Figure 5.23 shows the dynamic response during cooling from hottest temperature to coldest temperature when is applied 24 V to the Peltier assembly module. The data was imported to MATLAB to plot the curve.

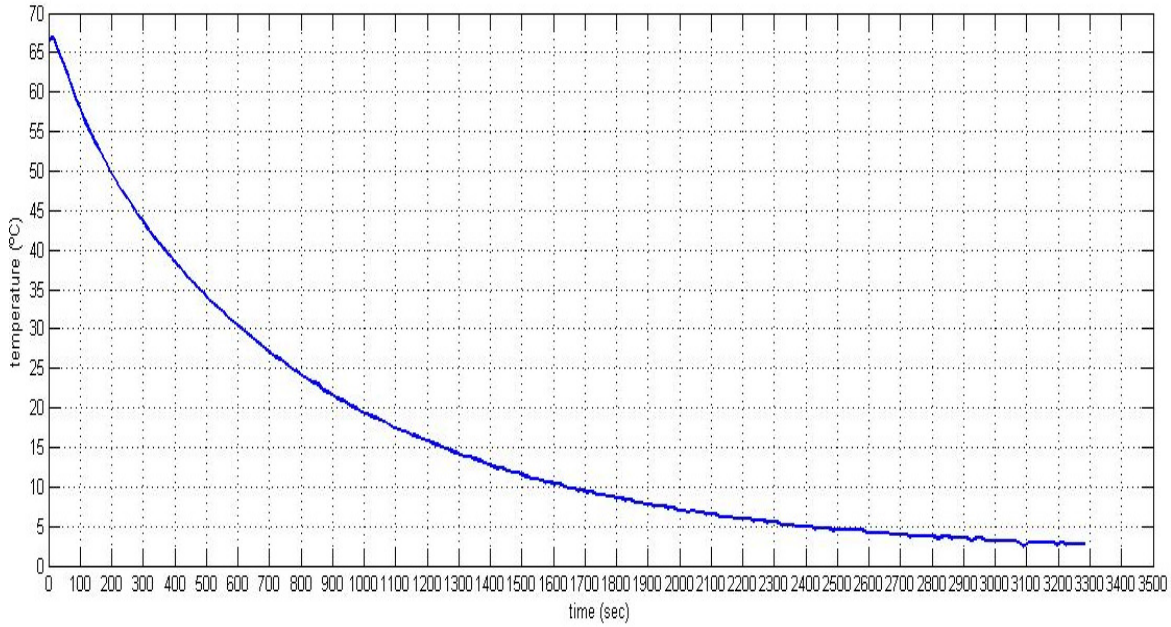


Figure 5.23 Dynamic response of system during cooling from hottest to coldest temperature.

5.5 APPLICATION SETUP AND RESULT ANALYSIS

To evaluate the best control type and method to apply to the heating process and cooling process it is analyzed the step responses using the data-logger comparing with best fitting first order transfer function.

Figure 5.24 shows the heating transfer function by measuring temperature blue color and first order transfer function fitting with red color obtained with MATLAB, corresponding to the following transfer function with obtained K and τ parameters.

- K=69 -24 =45
- τ corresponds to the time where the curve reaches 63% of the difference between 24ºC and 69 ºC. From the data-logger curve we get τ= 650 s.

$$G(s) = \frac{K}{\tau s + 1} = \frac{45}{650s + 1} \tag{5.4}$$

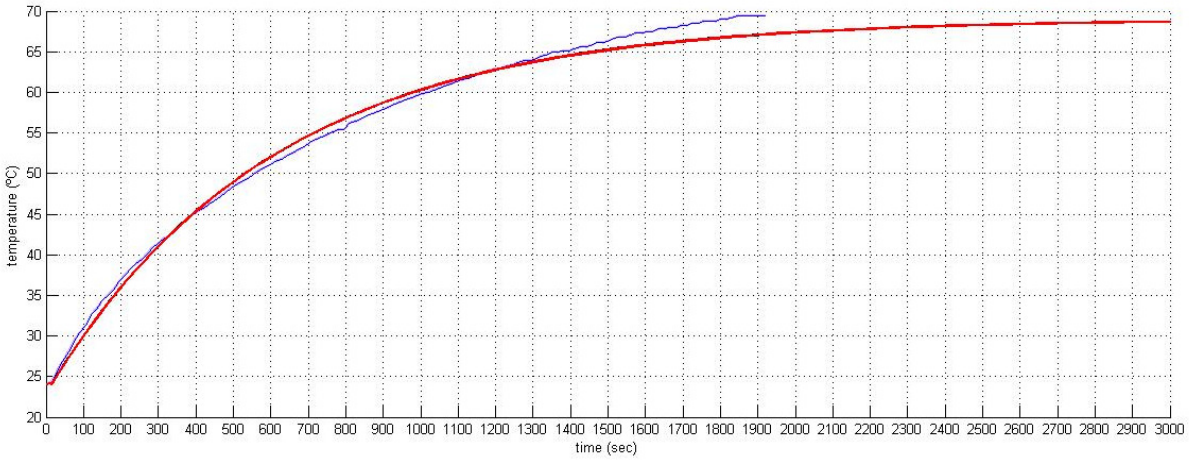


Figure 5.24 Dynamic response of system during heating and approximated first order transfer function.

Figure 5.25 shows the cooling transfer function by measuring temperature with blue color and correspondent first order transfer function fitting with red color obtained with MATLAB, corresponding to the following transfer function with obtained K and τ parameters.

- K=21.7 - 3.7 = 18
- τ corresponds to the time where the curve reaches 63% of the difference between 21.7ºC and 3.7 ºC. From the data-logger curve we get $\tau = 450$ s.

$$G(s) = \frac{K}{\tau s + 1} = \frac{18}{450s + 1} \tag{5.5}$$

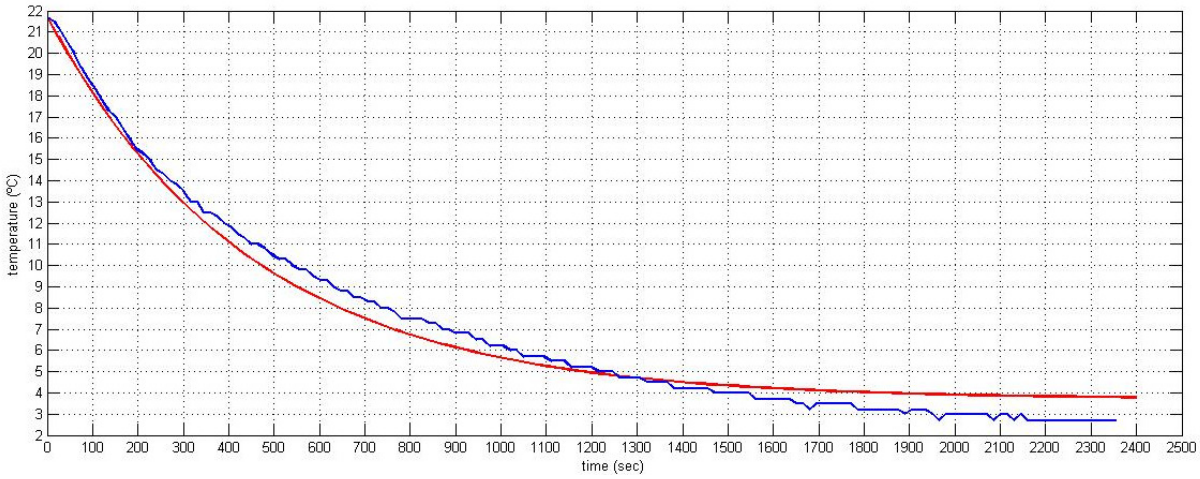


Figure 5.25 Dynamic response of system during cooling and approximated first order function.

The process responses are very slow and have nonlinearities. It is implemented a PI controller as it is not expected overshoot on the response and in this case it is not necessary the

use of derivative. It was used a simple manual tuning method commonly applied in the industry. It can be described in two steps as follows:

- Set and increase the proportional gain until get a small steady state error.
- Set and increase if necessary the integral gain to reduce to the minimum the steady state error.

For the heating process, it was performed the experiments according Table 5.1, applying the manual tuning method to the PI controller with different gain values.

Table 5.1 Experiment results during PI tuning for the heating process.

Experiment	Kp	Ki	Setpoint temperature	Reached temperature
1	6	0	50 ºC	35,5 ºC
2	15	0	50 ºC	42,6 ºC
3	30	0	50 ºC	47,4 ºC
4	30	10	50 ºC	49,9 ºC
5	30	20	50 ºC	50,1 º

Figure 5.26 shows the system responses with PI tuning method for different Kp and Ki gain values during heating process.

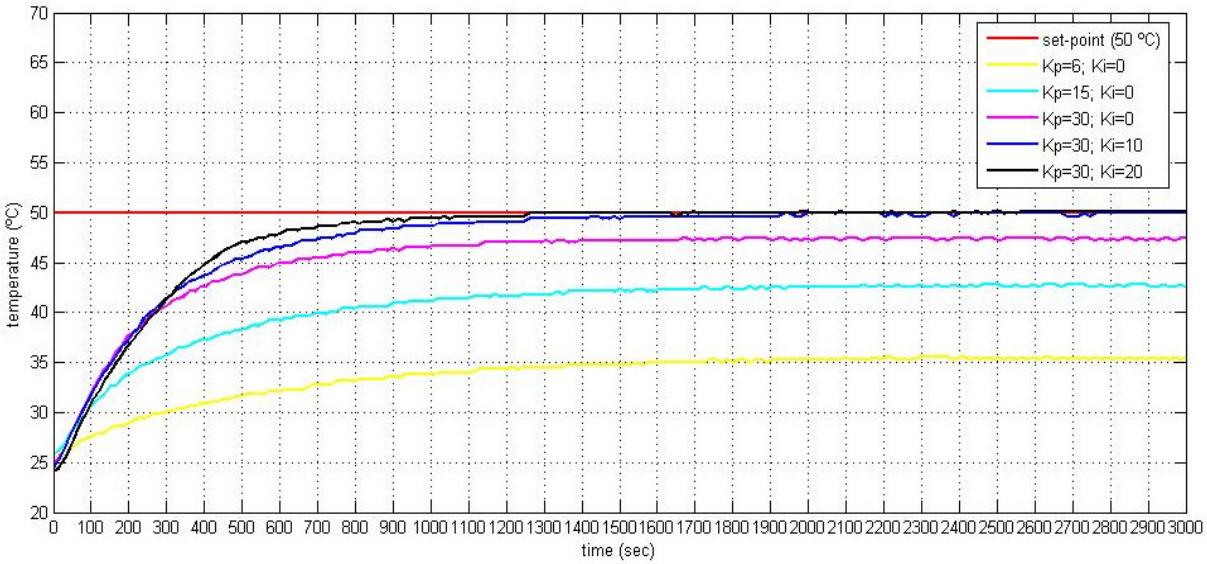


Figure 5.26 Dynamic responses of system during tuning method for the heating process.

The chosen values for the PI gain parameters that give a better response are:

- Kp =30
- Ki =20

Figure 5.27 shows the process response for different temperature setpoints during heating process.

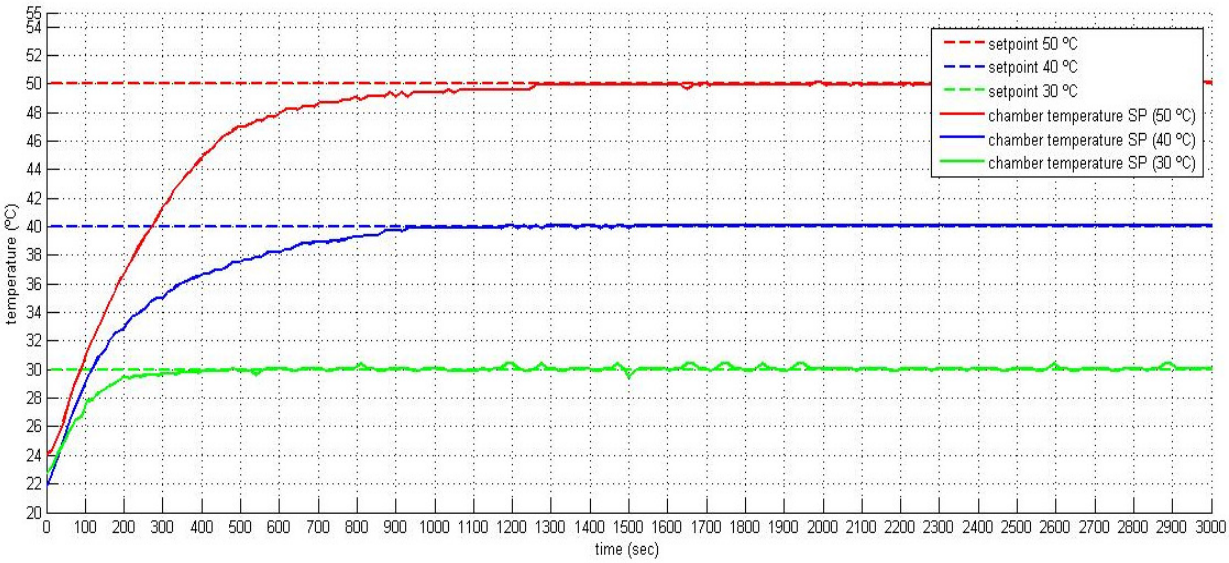


Figure 5.27 Dynamic responses of system for different temperature setpoints for heating process.

For the cooling process, it was performed the experiments according Table 5.2, applying the manual tuning method to the PI controller with different gain values.

Table 5.2 Experiment results during PI tuning for the cooling process.

Experiment	Kp	Ki	Setpoint temperature	Chamber stabilized temperature
1	20	0	10 °C	15,5 °C
2	30	0	10 °C	14,5 °C
3	50	0	10 °C	13,3 °C
4	70	0	10 °C	12,5 °C
5	70	10	10 °C	10,5 °C
6	70	20	10 °C	10,0 °C

Figure 5.28 shows the system responses with PI tuning method for different Kp and Ki gain values during cooling process.

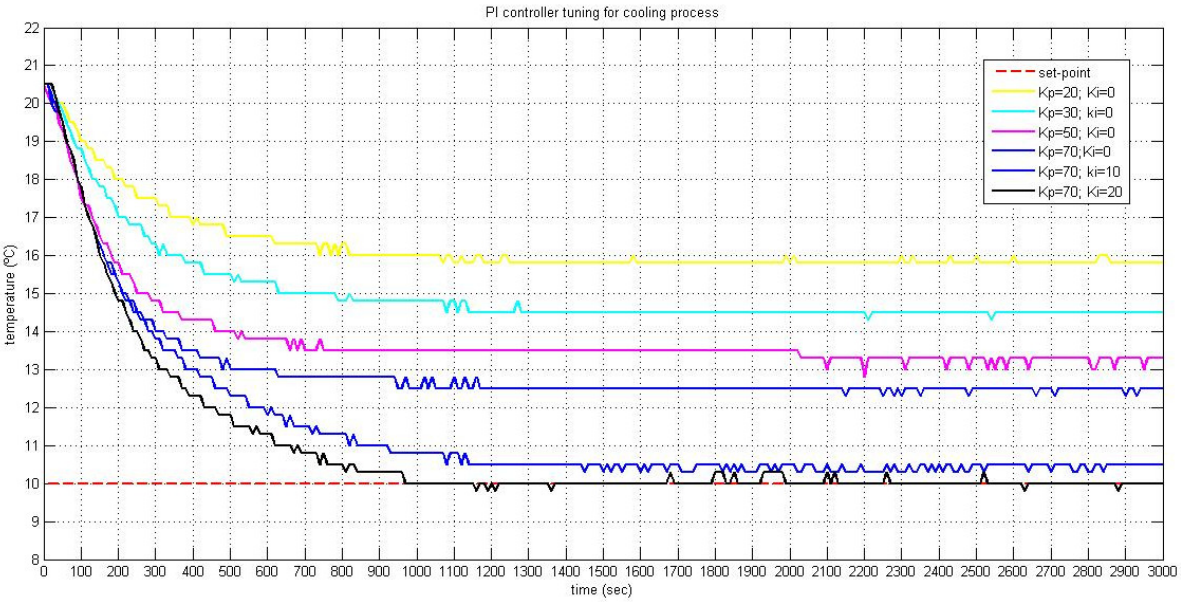


Figure 5.28 Dynamic responses of system during tuning method for the cooling process.

The chosen values for the PI gain parameters that give a better response are according the black response curve of Figure 5.28:

- Kp =70
- Ki =20

Figure 5.29 shows the process response for different temperature setpoints during cooling process.

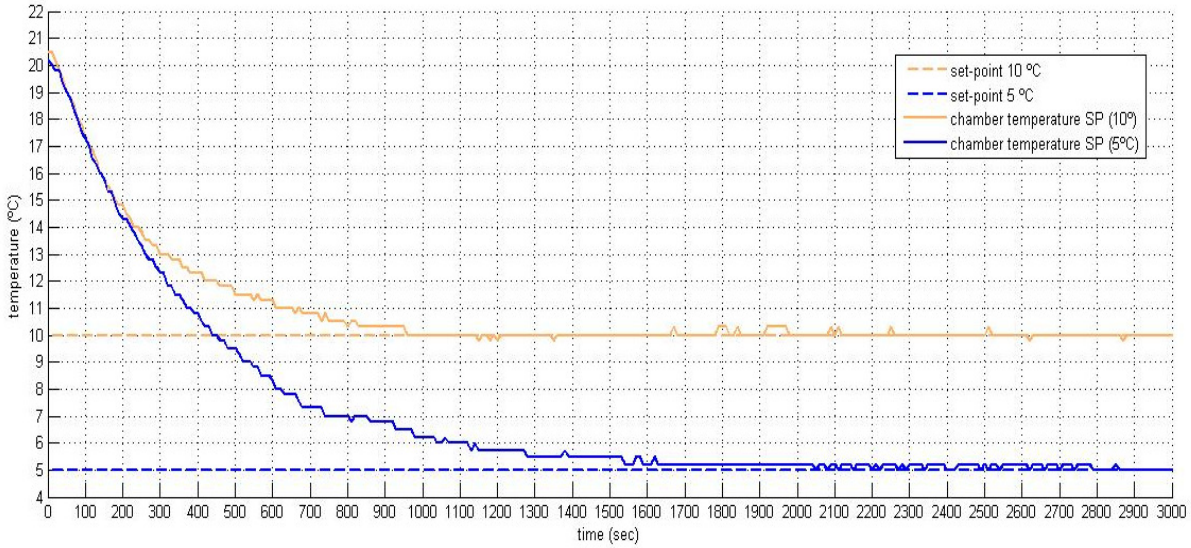


Figure 5.29 Dynamic responses of system for different temperature setpoints for cooling process.

After getting results with different setpoints, it is possible to conclude that the PI controller design used for the heating process and PI design for cooling process fulfill the control requirement of stabilizing temperature around the setting temperature. Figure 5.30 shows the final setup of implemented system and instrumentation.

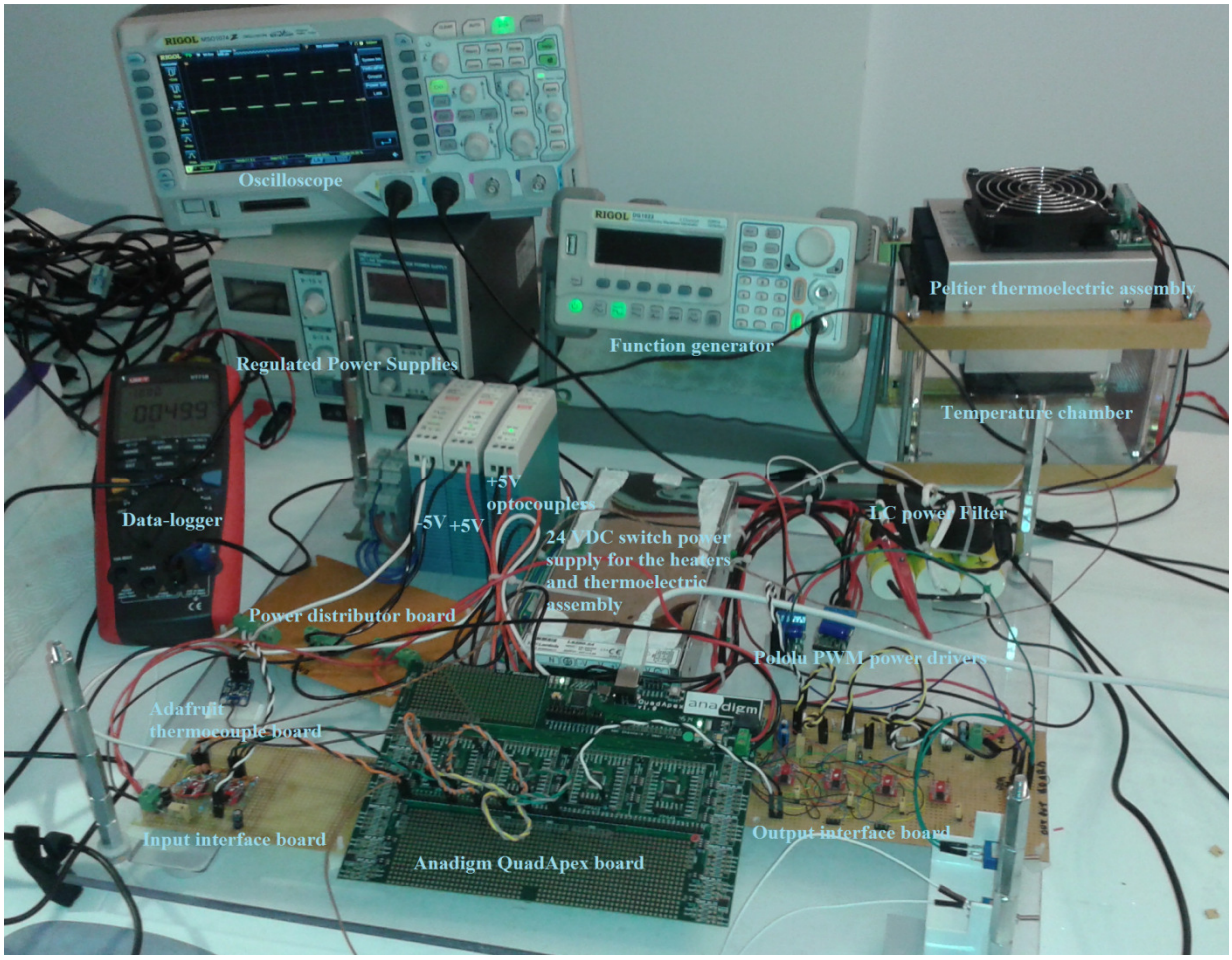


Figure 5.30 Hardware development and instrumentation.

5.6 DISCUSSION

The hardware implemented to control temperature chamber was tested with success as shows the responses dynamic curves obtained by the data-logger for different setpoints.

Taking into consideration that heating and cooling processes are very slow according dynamic responses and the existence of nonlinearities and noise in the system, it was selected a PI mode controller to implement on FPAA/dpASP.

It was applied a simple manual tuning method instead of heuristic method like Ziegler-Nichols or other, because the process dynamic response does not fit well on first order transfer function with delay. Also, it is not possible to put the system oscillating in the critical point for instability according second method of Ziegler-Nichols.

It should be taken into consideration that a small increment of 2.5 mV on the reference voltage corresponds to 1 ºC of increased temperature which can very easily create an error during trimer adjustment of the setpoint.

The electronic hardware involved on the closed-loop control system has the expected behavior, specially the power LC filter of PWM driver for the Peltier assembly which gives very low ripple DC voltage on output.

The new AnadigmQuadApex board released in April is very flexible in terms of configuration of the FPAA/dpASP interconnected in chain. Also, the layout disposal I/O pins facilitates the oscilloscope monitoring and the inclusion of micro-switches to route some I/O pins between IC FPAAs makes easier the signal routing setup.

6 CONCLUSION

This chapter finalizes this work, summarizing conclusions and pointing out aspects to be developed in future work.

After finished this work, it is possible to say that there are mainly two technologies and solutions for FPAA manufacturing. Most of academic FPAA projects are based on the continuous time principle basically using OTAs while the currently commercially available IC devices are made by Anadigm and work on discrete time SC technological principle. One reason for the popularity of SC technology is the fact that SC circuits allow to obtain a range of parameter change by means of the switching clock frequency. Academic projects are more concentrated in CT technology because it provides higher bandwidth, necessary for image processing and wireless applications. The FPAA/dpASP technology is flexible and reduces the development time of systems for process signals on analog domain.

During this Thesis were used two types of boards (AnadigmApex and AnadigmQuad Apex). Both boards have the same third generation FPAA/dpASP device and were used their resources to implement PID control, filters and signal conditioning applications.

The implementation of control blocks uses many resources which require several FPAA/dpASPs connected in a chain by SPI protocol. As more complex are the systems then more devices interconnected will be necessary as the Anadigm third generation FPAA/dpASP has only four CABs available per device. However, the use of FPAA/dpASPs in analog

projects enables the reduction of hardware to implement the circuits and flexibility to reprogram on the fly which means change configuration without make reset to the device.

The dpASP third generation device from Anadigm was used to emulate transfer functions and PID controller with several different settings with oscilloscope results similar with those obtained using MATLAB which is very important to validate the used models. However it is important to note, that it was necessary to do always a previous model analysis using Anadigm Designer simulator to check possible saturation on the CAMs specially on proportional and integral gain blocks or noise appearance on differential blocks or half cycle sum/dif CAMS. To avoid this noise it is necessary to filter the signals using bilinear transfer functions configured with proper corner frequency. Also it was necessary to use small amplitude input signals to avoid saturation as third generation AnadimApex device supply voltage is 3 V and internal ground VMR is 1.5 V, instead of previous second generation AnadigmVortex device which uses 5 V supply technology and VMR of 2 V giving a bigger analog amplitude voltage working range.

The capabilities of dpASP used in the control application shown flexibility and it is a fast method to implement controller due to fact that is possible to do several simulations with different settings and download on the fly in few milliseconds new configurations without making reset or modify the hardware which normally is time consuming. On the other hand, it is still necessary to implement external hardware to make the input and output signal interface to the I/O pins which shown some problems and concerns to avoid noise injection especially on the input pins that affects the response of the implemented models.

Also, the range available to select the Ki from integration CAM and Kd from differential CAM is very limited to small values, due to the fact that on chip FPAA matrix selector of available capacitors have very small values. To overcome this technological limitation and as improvement for future work, could be implemented externally to the device necessary capacitors to implement integrators and differentiators with a higher range for Ki and Kd setting parameters, increasing the controllability with more efficiency for slower processes.

Future work developments could be done using mixed technology of FPAA and FPGA interconnected by SPI bus or ADC/DAC converters. FPGA can implement the logic I/O control system and FPAA/dpASP can implement analog signal system, signal processing and signal conditioning. This mixed technology implements the equivalent system of a reconfigurable SOC. Usage of dpASPs permits the easy replication of controllers on same hardware which is a

great advantage where the design of fault tolerant control systems is mandatory due to critical applications, as well in conjunction with FPGAs to generate logic control.

As well, for cooling and control temperature of CPUs and power electronic semiconductor devices with direct contact Peltier modules and semiconductor parameter testing, it is possible to use Peltier air-to-air or direct-air temperature controlled devices to measure and characterize semiconductor electrical DC and AC parameters dependent from exposed temperature.

Future work and developments can be done applying the FPAA/dpASP technology including design high level language (Visual C++ or Visual C#) applications based on code generation by Anadigm Designer for Visual Studio, which can implement graphical interfaces to change the CAM setting parameters of dpASPs and on the fly.

Applications for auto-tuning algorithms using PID controllers can be developed using the PIC32 mounted on AnadigmQuadApex board and the interface with high level application (Visual C++ and C#).

Regarding practical applications of controlled temperature chambers, it is possible to develop small labs in locations where it is impossible to transport and use heavy gas compression cooling systems or heating with conventional heaters. Also, cooling controlled temperature chambers for wide range of scientific and technological evaluations. Temperature control of cooling liquid using air-liquid Peltier assembly modules or controlling temperature of air flow in pipes with small diameters are also possible.

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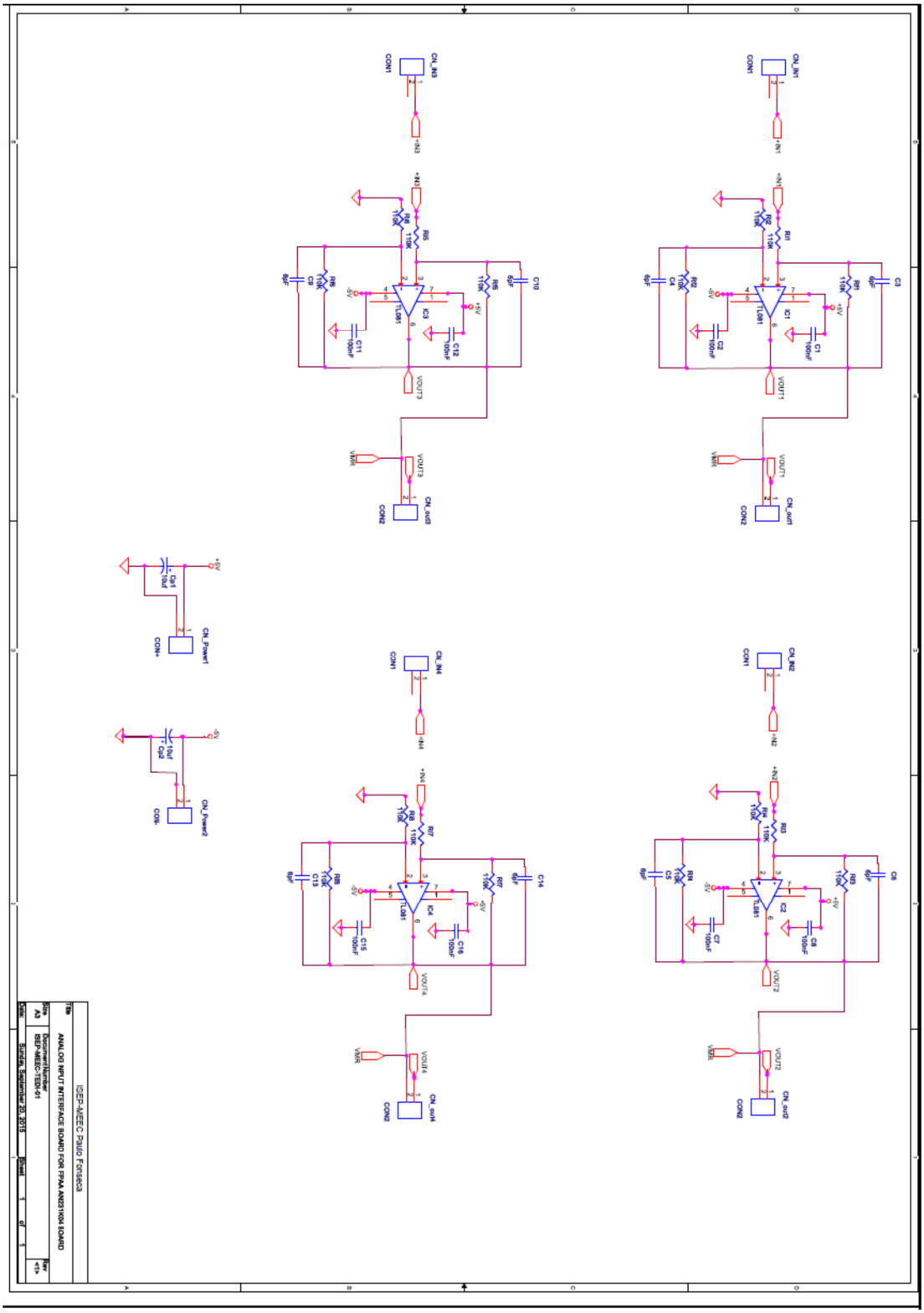
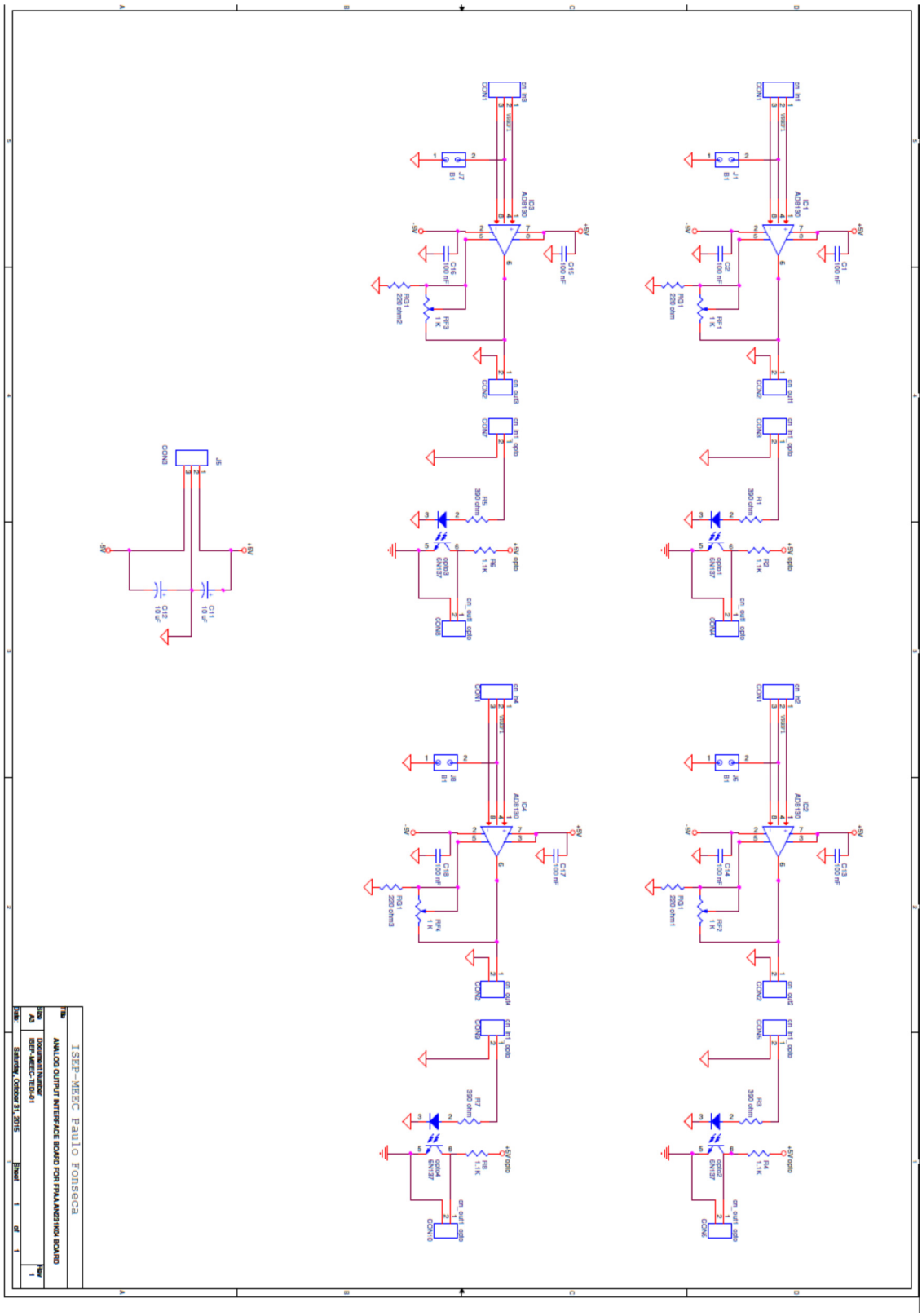
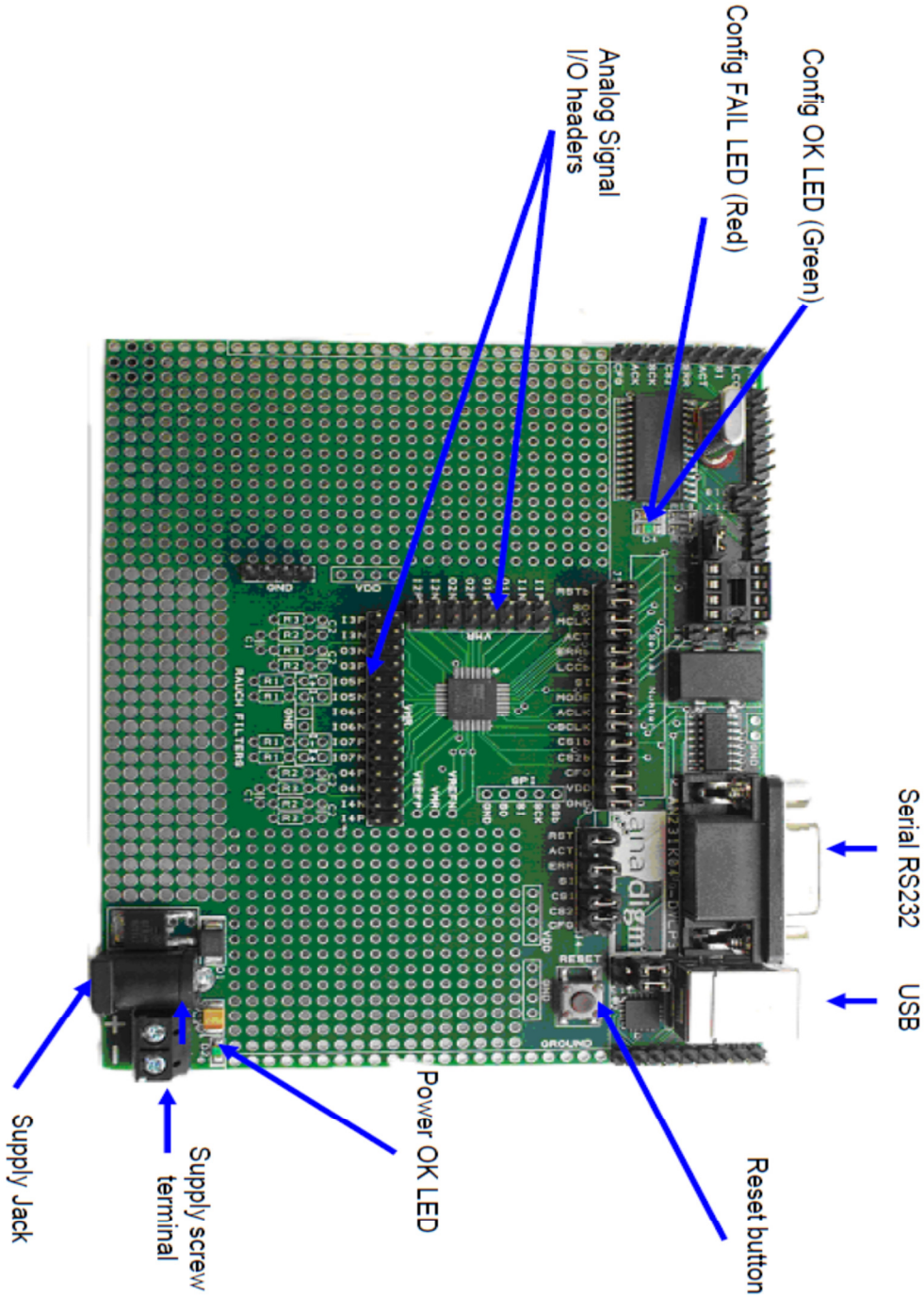
Appendix A. Analog input interface board

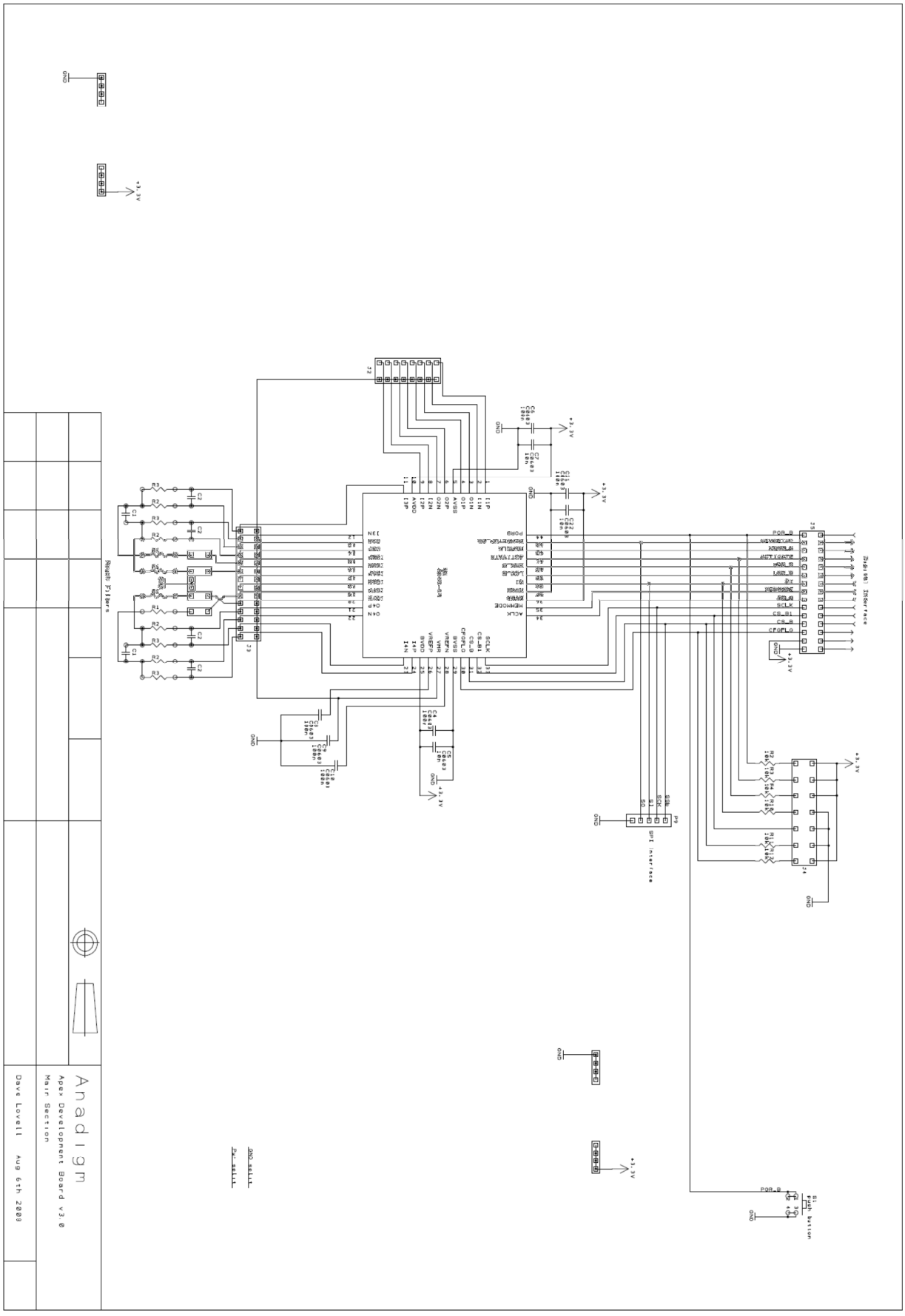


Appendix B. Analog output interface board



Appendix C. AN231K04-DVLP3 – AnadigmApex development board schematics [34]

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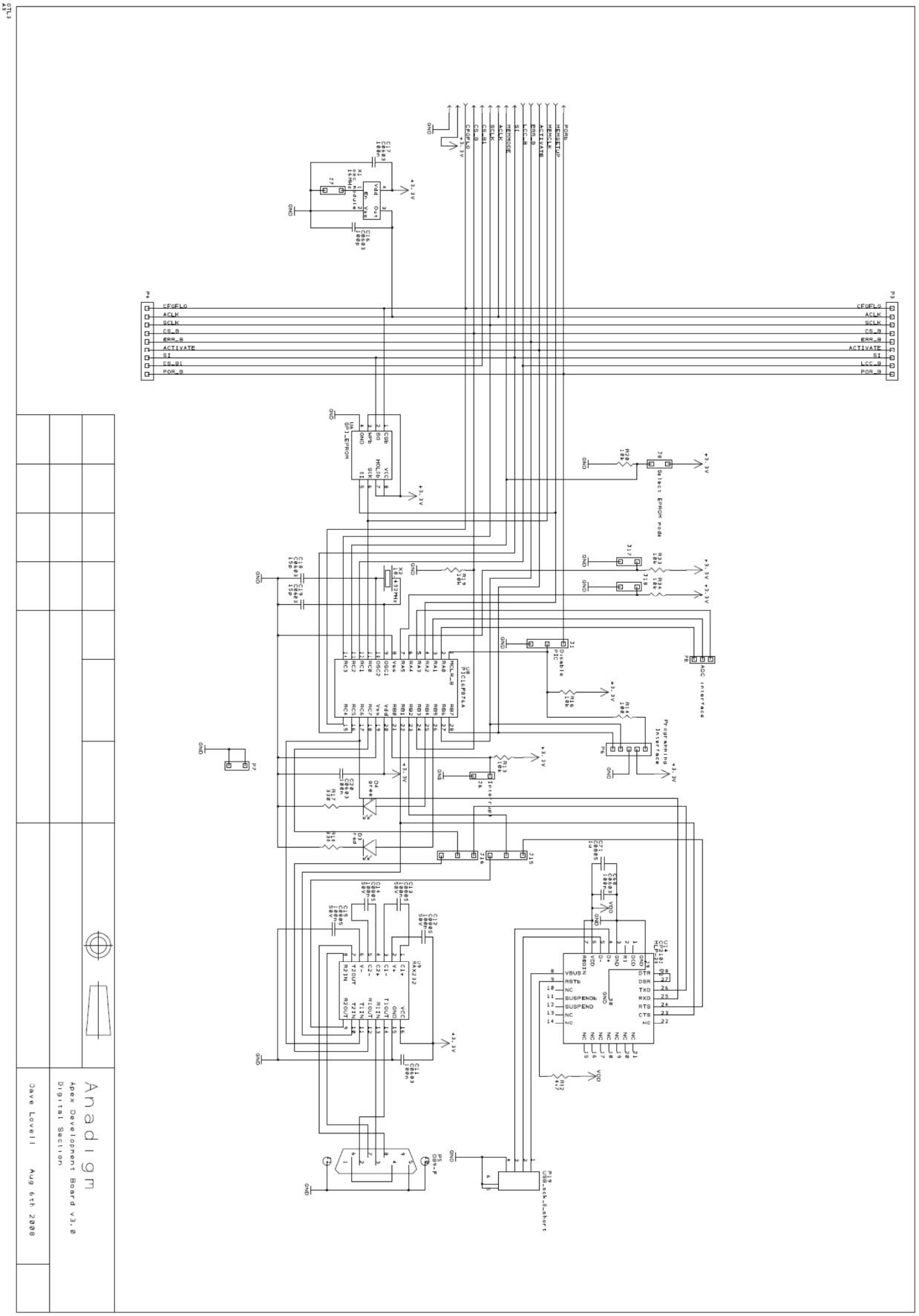
Apex Development Board v3.0
Main Section
Dave Lovell
Aug 6th 2008
Anadigm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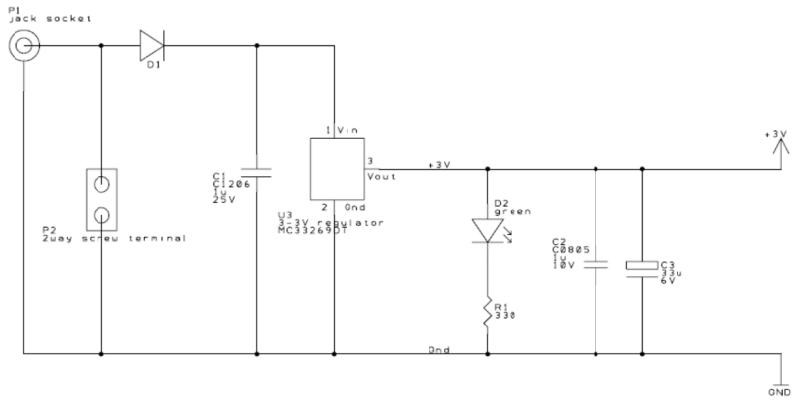
Aug 6th 2008



Anadigm

Apex Development Board v1.0

Power Section

Dave Lovell July 8th 2005

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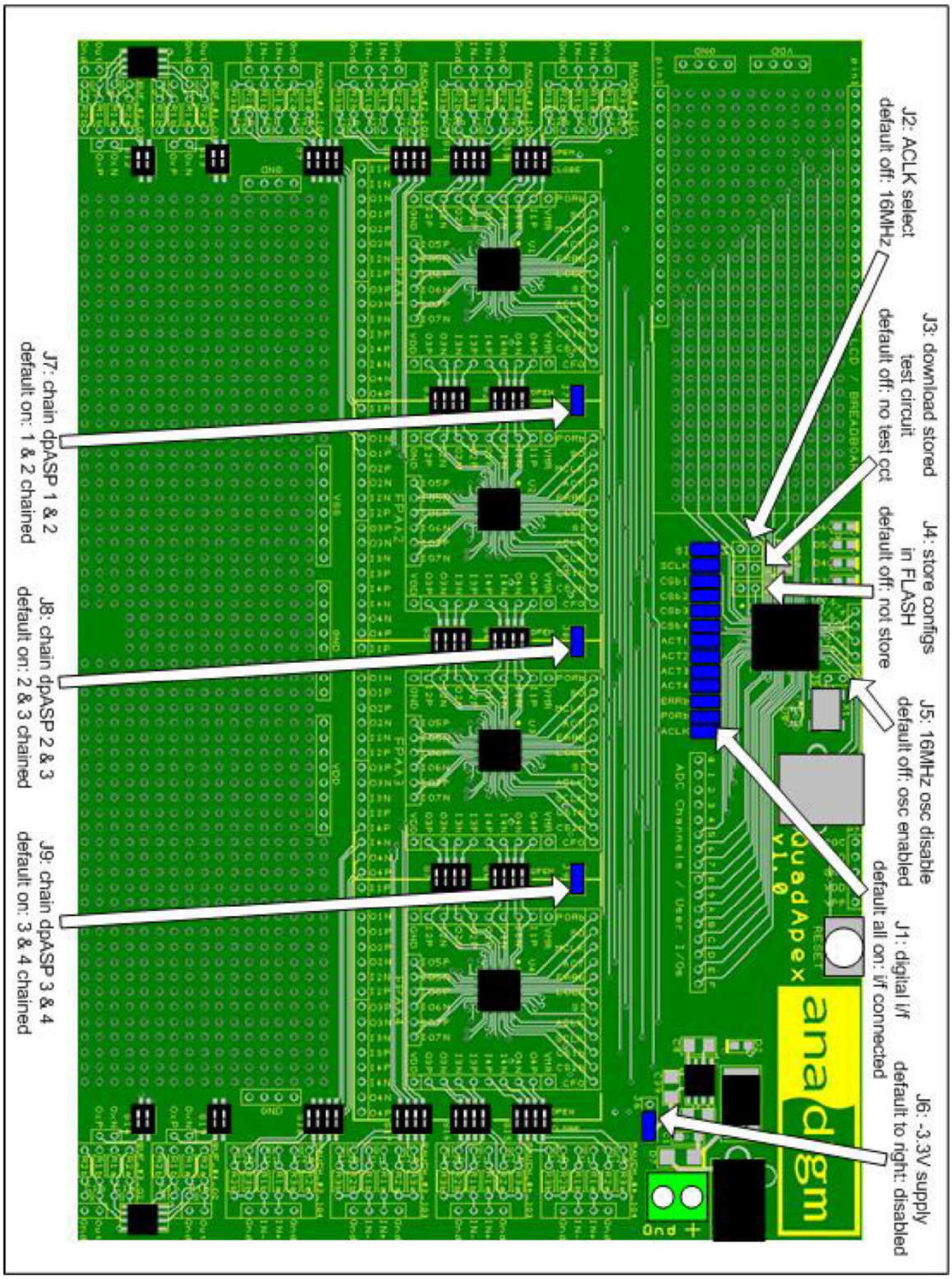
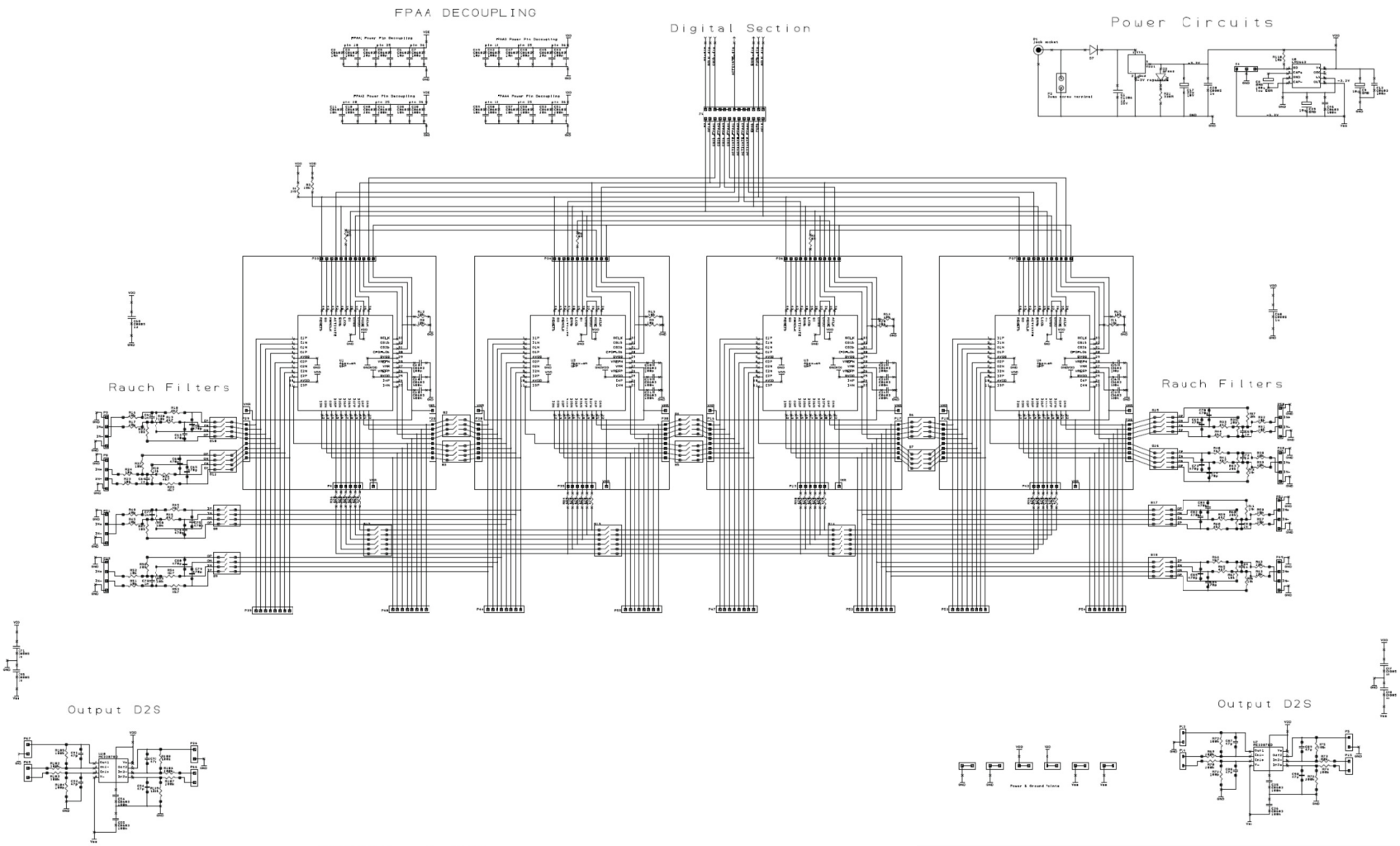
Appendix D. Anadigm QuadApex development board schematics [46]

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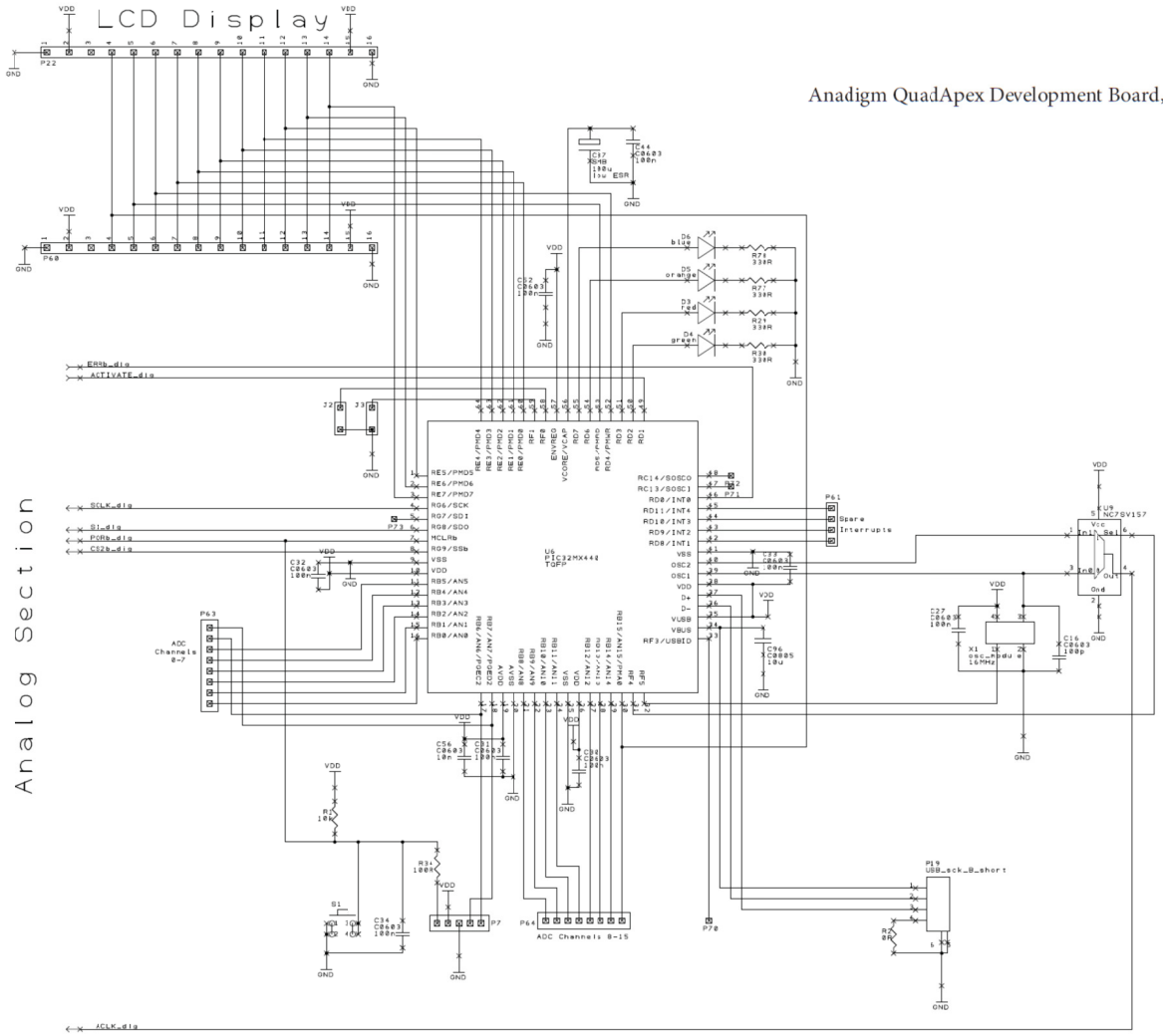
Output D2S



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Appendix E. Peltier assembly module physical principles, advantages, disadvantages and applications

The physical principles which modern thermoelectric coolers are based actually date back to the early 1800's, although commercial TEC modules were not available until almost 1960.

The first important discovery relating to thermoelectricity occurred in 1821 when a German scientist, Thomas Seebeck, found that an electric current would flow continuously in a closed circuit made up of two dissimilar metals provided that the junctions of the metals were maintained at two different temperatures. Seebeck did not actually comprehend the scientific basis for his discovery, however, and falsely assumed that flowing heat produced the same effect as flowing electric current.

In 1834, Jean Peltier, while investigating the "Seebeck effect," found that there was an opposite phenomenon whereby thermal energy could be absorbed at one dissimilar metal junction and discharged at the other junction when an electric current flowed within the closed circuit.

Twenty years later, William Thomson (eventually known as Lord Kelvin) issued a comprehensive explanation of the Seebeck and Peltier effects and described their interrelationship. At the time, however, these phenomena were still considered to be mere laboratory curiosities and were without practical application.

In the 1930's Russian scientists began studying some of the earlier thermoelectric work in an effort to construct power generators for use at remote locations throughout the country. This Russian interest in thermoelectricity eventually caught the attention of the rest of the world and inspired the development of practical thermoelectric modules. Today's thermoelectric coolers make use of modern semiconductor technology whereby doped semiconductor material takes the place of dissimilar metals used in early thermoelectric

experiments. The Seebeck, Peltier, and Thomson effects, together with several other phenomena, form the basis of functional TEC modules.

A practical thermoelectric cooler consists of two or more elements of semiconductor material that are connected electrically in series and thermally in parallel. These thermoelectric elements and their electrical interconnects typically are mounted between two ceramic substrates. The substrates serve to hold the overall structure together mechanically and to insulate the individual elements electrically from one another and from external mounting surfaces. After integrating the various component parts into a module, thermoelectric modules ranging in size from approximately 2.5-50 mm (0.1 to 2.0 inches) square and 2.5-5mm (0.1 to 0.2 inches) in height may be constructed.

Both N-type and P-type Bismuth Telluride thermoelectric materials are used in a thermoelectric cooler. This arrangement causes heat to move through the cooler in one direction only while the electrical current moves back and forth alternately between the top and bottom substrates through each N and P element. N-type material is doped so that it will have an excess of electrons (more electrons than needed to complete a perfect molecular lattice structure) and P-type material is doped so that it will have a deficiency of electrons (fewer electrons than are necessary to complete a perfect lattice structure). The extra electrons in the N material and the "holes" resulting from the deficiency of electrons in the P material are the carriers which move the heat energy through the thermoelectric material. Most thermoelectric cooling modules are fabricated with an equal number of N-type and P-type elements where one N and P element pair form a thermoelectric "couple." The module illustrated on next Figure has two pairs of N and P elements and is termed a "two-couple module".

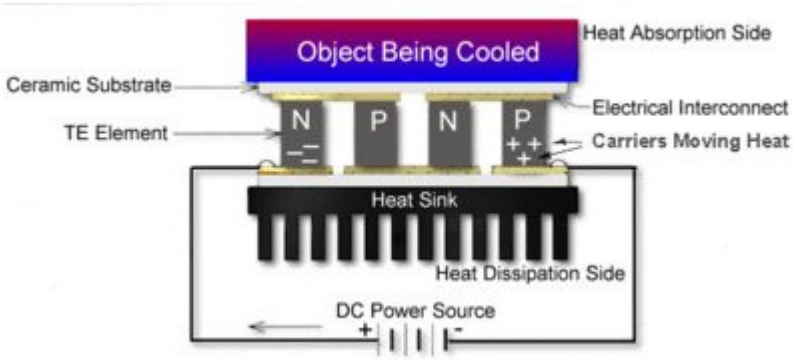

Figure E.1 Diagram of a direct-to-air thermoelectric cooler [42].

Heat flux (heat actively pumped through the thermoelectric module) is proportional to the magnitude of the applied DC electric current. By varying the input current from zero to maximum, it is possible to adjust and control the heat flow and temperature.

ADVANTAGES OF THERMOELECTRIC COOLING

- The use of thermoelectric modules often provides solutions, and in some cases the ONLY solution, to many difficult thermal management problems where a low to moderate amount of heat must be handled. While no one cooling method is ideal in all respects and the use of thermoelectric modules will not be suitable for every application, TE coolers will often provide substantial advantages over alternative technologies. Some of the more significant features of thermoelectric modules include:
- No moving parts: A TE module works electrically without any moving parts so they are virtually maintenance free.
- Small size and weight: The overall thermoelectric cooling system is much smaller and lighter than a comparable mechanical system. In addition, a variety of standard and special sizes and configurations are available to meet strict application requirements.
- Ability to cool below ambient: Unlike a conventional heat sink whose temperature necessarily must rise above ambient, a TE cooler attached to that same heat sink has the ability to reduce the temperature below the ambient value.
- Ability to heat and cool with the same module: Thermoelectric coolers will either heat or cool depending upon the polarity of the applied DC power. This feature eliminates the necessity of providing separate heating and cooling functions within a given system.
- Precise temperature control: With an appropriate closed-loop temperature control circuit, TE coolers can control temperatures to better than +/- 0.1°C.
- High reliability: thermoelectric modules exhibit very high reliability due to their solid state construction. Although reliability is somewhat application dependent, the life of typical TE coolers is greater than 200,000 hours.

- Electrically "quiet" operation: Unlike a mechanical refrigeration system, TE modules generate virtually no electrical noise and can be used in conjunction with sensitive electronic sensors. They are also acoustically silent.
- Operation in any orientation: TEs can be used in any orientation and in zero gravity environments. Thus they are popular in many aerospace applications.
- Convenient power supply: TE modules operate directly from a DC power source. Modules having a wide range of input voltages and currents are available. Pulse Width Modulation (PWM) may be used in many applications.
- Spot cooling: with a TE cooler. It is possible to cool one specific component or area only, thereby often making it unnecessary to cool an entire package or enclosure.
- Ability to generate electrical power: When used "in reverse" by applying a temperature differential across the faces of a TE cooler, it is possible to generate a small amount of DC power.
- Environmentally friendly: Conventional refrigeration systems cannot be fabricated without using chlorofluorocarbons or other chemicals that may be harmful to the environment. Thermoelectric devices do not use or generate gases of any kind.

DISADVANTAGES OF THERMOELECTRIC COOLING

- Able to dissipate limited amounts of heat flux.
- Condensation is another potential dangerous problem, occurring if components are cooled too much below the ambient temperature.
- Not as efficient, in terms of performance as gas-compression systems.

APPLICATIONS

Thermoelectric Assemblies are used in a wide range of applications to stabilize the temperature of sensitive electronic components or cool devices and compartments below ambient temperature.

On telecommunications, cooling below ambient is necessary to extend life of batteries in wireless base stations. Temperature stabilization is required to maintain peak performance of laser diodes. Colling telecom Enclosures, battery backup systems

On Medical sector, temperature stabilization is required to obtain a high image resolution. Cooling reagent chambers below ambient is critical to extend life of reagents and

keep replacement costs down. Rapid thermal cycling is crucial to speed up DNA amplification. Clinical diagnostics and analytical instrumentation

On industrial & instrumentation, temperature stabilization is critical to maintain industrial lasers at peak performance and allows high end printing systems to produce high quality prints at high run rates. Also, high powered projectors, metrology instrumentation, industrial laser systems.

On food & beverage, the temperature control is crucial to keep food fresh and beverages cold. Small refrigerators, portable food containers.

Appendix F – Temperature sensor interface circuit for FPAA/dpASP with three thermocouples