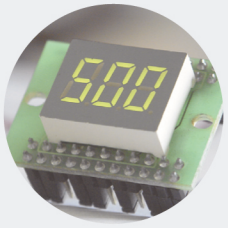
INSTITUTO SUPERIOR DE ENGENHARIA DO PORTO
MESTRADO EM ENGENHARIA ELECTROTÉCNICA E DE COMPUTADORES






Communication Controller Design for an Electric Vehicle Charging Station

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Communication Controller Design for an Electric Vehicle Charging Station

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This dissertation partially satisfies the requirements of the Thesis/Dissertation course of the program Master in Electrical and Computer Engineering, Specialization Area of Autonomous Systems.

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Abstract

The recent surge in electric mobility for road vehicles is a direct response to the substantial pollution generated throughout the lifespan of combustion vehicles. Consequently, to combat this issue and contribute to a greener and more sustainable planet, the establishment of a robust network of Electric Vehicle Supply Equipment (EVSE) is imperative. Among the various available charging modes and their respective protocols, the *Combined Charging System* (CCS) protocol stands out in Europe as the most used, as it is very robust and facilitates both Alternating Current (AC) and Direct Current (DC) fast charging. For DC charging under this protocol, an Electric Vehicle (EV) interface communication controller on the charger side is essential for enabling communication between the EV and the Supply Equipment.

This thesis outlines the development of a Supply Equipment Communication Controller (SECC) circuit that complies with the specified standards of the CCS protocol. The primary function of the controller is to establish a bidirectional communication interface between the charger central unit and the EV. This is achieved through *Power-line Communication* (PLC) and a low-level Pulse-width Modulation (PWM) signal transmitted in the same line, for communication with the vehicle, while communication with the charger processing controllers is accomplished via *Controller Area Network* (CAN).

After an extensive analysis and comparison, the most crucial *System on a Chip* (SoC) selected for the project are introduced. These include the Microcontroller Unit responsible for the controller processing and the intricate PLC chip, which manages the communication interface with the EV. Subsequently, the remaining designed and implemented circuits are presented, encompassing voltage supply circuits, communication interface circuits, and auxiliary circuits required for the communication with the electric vehicle.

Finally, circuit simulations were conducted on specific parts of the circuit to ensure overall compliance with the system requirements.

Keywords: Supply Equipment, Electric Vehicle, Electric Mobility, Supply Equipment Communication Controller (SECC), Power-line Communication (PLC), Controller Area Network (CAN), Circuit Simulation.

Resumo

Nos dias de hoje, é altamente difícil ignorar a revolução da mobilidade elétrica. A exponencial produção de VEs pretende dar responde à poluição gerada pelos veículos a combustão. Para combater este problema e promover um planeta mais verde e sustentável, é crucial estabelecer uma rede robusta de carregadores elétricos que satisfaça a alta procura de carregamentos rápidos de VE. Entre os diversos modos de carregamento, o *Combined Charging System* (CCS) destaca-se na Europa pela sua robustez e capacidade de suportar tanto carregamentos em Corrente Alternada (CA) como em Corrente Contínua (CC). Para veículos que possuam o protocolo CCS, um controlador de comunicação na interface do carregador com o veículo elétrico é essencial para a troca de informações entre o Veículos Elétricos (VE) e o equipamento de fornecimento de energia.

O presente relatório descreve o projeto de um controlador de comunicação para equipamentos de fornecimento de energia que cumpre com as normas especificadas pelo protocolo CCS. A função principal do controlador é estabelecer uma interface de comunicação bidirecional entre a unidade central do carregador e o veículo. Isto é alcançado através de *Power-line Communication* (PLC) e um sinal de modulação por largura de pulso (*Pulse-width Modulation* (PWM)) transmitidos na mesma linha para comunicação com o veículo, enquanto a comunicação com as unidades de processamento do carregador é realizada via *Controller Area Network* (CAN).

Após uma intensa análise comparativa, são selecionados os *System on Chip* (SoC) para o projeto. Estes incluem o Microcontrolador, responsável pelo processamento do controlador, e o chip PLC, responsável pela interface de comunicação com o VE. Subsequentemente, são apresentados os restantes circuitos projetados e implementados, tais como os circuitos de alimentação (em tensão), circuitos das interfaces de comunicação e circuitos auxiliares necessários para a comunicação com o VE.

Finalmente, é detalhada a fase final do projeto, que envolveu a realização de simulações de blocos específicos do circuito para garantir a conformidade do sistema de acordo com as suas especificações.

Palavras-Chave: Veículos elétricos, Mobilidade elétrica, Controlador de comunicação de carregadores de veículos elétricos, Carregador de veículos elétricos, *Power-line Communication* (PLC), *Controller Area Network* (CAN), Simulação de circuitos.

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List of Acronyms

AC	Alternating Current
ADC	Analog-to-Digital Converter
BGA	Ball Grid Array
CA	Corrente Alternada
CAN	Controller Area Network
CAN FD	Controller Area Network Flexible Data-Rate
CANH	CAN High
CANL	CAN Low
CC	Corrente Contínua
CCS	Combined Charging System
CHAdeMO	CHArge de MOve
CMK	Common Mode Choke
CMS	Cable Management System
COTS	Commercial-off-the-shelf
CP	Control Pilot
CPO	Charge Point Operator
DC	Direct Current
EDA	Electronic Design Automation
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EU	European Union
EV	Electric Vehicle

EVSE	Electric Vehicle Supply Equipment
GUI	Graphical User Interface
HMI	Human Machine Interface
HPGP	HomePlug Green PHY
IBIS	Input/Output Buffer Information Specification
IC	Integrated Circuit
IEC	International Electrotechnical Commission
ISEP	Instituto Superior de Engenharia do Porto
JTAG	Joint Test Action Group
LED	Light-Emitting Diode
MAC	Media Access Controller
MCU	Microcontroller Unit
NACS	North American Charging Standard
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
PHY	Physical Layer
PLC	Power-line Communication
PP	Proximity Pilot
PTC	Positive Temperature Coefficient
PWM	Pulse-width Modulation
QFP	Quad Flat Package
RISC	Reduced Instruction Set Computing
RMII	Reduced Media Independent Interface
RX	Receive
SDRAM	Synchronous Dynamic Random-Access Memory
SECC	Supply Equipment Communication Controller

SoC	System on a Chip
SOTA	State Of The Art
SPI	Serial Peripheral Interface
SPICE	Simulation Program with Integrated Circuit Emphasis
TP	Test Point
TVS	Transient-voltage-suppression
TX	Transmit
UART	Universal Asynchronous Receiver-Transmitter
USA	United States of America
USB	Universal Serial Bus
VE	Veículos Elétricos

List of Symbols

Symbol	Description	Units
C	Capacitance	F
E	Energy	J
η	Efficiency	%
f	Frequency	Hz
I	Current	A
L	Inductance	H
P	Power	W
R	Resistance	Ω
s	Seconds	s
V	Voltage	V
Z	Impedance	Ω

Chapter 1

Introduction

This document reports the main results of a project carried out at i-charging, in the scope of a Master Thesis in Electrical and Computer Engineering at Instituto Superior de Engenharia do Porto (ISEP).

This introductory chapter provides a brief contextualization of the i-charging company and the project at stake. The "problem" is also defined, along with the objectives and high-level project architecture, the organization, and work methodology. Finally, the contributions of this Thesis and the document structure are presented.

1.1 Context

Due to the exponential increase in sales of Electric Vehicle (EV) in recent years, there is an imminent need to increase the number of Electric Vehicle Supply Equipment (EVSE). Thus, the expansion of electric charging networks capable of providing users with an easy, fast, and reliable charging experience has proven essential in promoting electric mobility and contributing to reducing fossil fuel usage, towards a greener future.

It is, therefore, the responsibility of EVSE manufacturers and EV Original Equipment Manufacturer (OEM)s to ensure interoperability between the charger and the vehicle without compromising the increase in charging speed, safety, and reliability.

Established in March 2019, i-charging [1] is headquartered in Porto, Portugal, with a branch office located in Georgia, USA. Its mission is to meet the ever-increasing need for electric vehicle charging stations (EVSEs), with a specific focus on fast-charging solutions. Recipient of the German Innovation Award 2022, German Design Awards 2022, and E-mobility Awards 2021, i-charging is driven by a set of fundamental principles encompassing sustainability, integrity, innovation, customer-centricity, trust, and commitment. The company primary objective is to design and produce cutting-edge solutions that drive the electric mobility industry forward and promote environmentally sustainable practices. With chargers all over the world, i-charging flagship products are:

- **blueberry:** a versatile 50 kW charging solution suitable for different charging protocols;
- **blueberry PLUS:** an upgraded version of blueberry, featuring external power unit(s) with a capacity of up to 900 kW;
- **blueberry CLUSTER:** tailored for high-demand charging locations, this solution supports simultaneously EV charging (up to 4), integrating a blueberry PLUS with external "satellites";
- **blueberry FUSION:** an all in one solution supporting up to 150 kW and capable of charging 2 EVs simultaneously without an external power unit.

Each product is equipped with a comprehensive Cable Management System (CMS). The latter listed solutions are depicted in Figure 1.1.

Figure 1.1: i-charging flagship products

Figure 1.2 identifies the primary blocks in most charging processes. The essential standards for providing electric power to not only electric road vehicles but also other forms of mobile electric transport, as well as the required communication

interface standards between the involved parties, are delineated within these blocks. Compliance with these standards must be guaranteed by meeting all applicable requirements.

Figure 1.2: Electric mobility ecosystem

Here is a brief definition of each block displayed in Figure 1.2:

- **Eletric Vehicle:** an EV refers to any vehicle powered by one or more electric motors, relying on rechargeable batteries for energy storage[1] [2];
- **Electric Vehicle Supply Equipment:** an EVSE refers to the infrastructure necessary for charging electric vehicles on AC and DC mode. This includes charging stations, connectors, power management systems, and associated software[2] [3];
- **Charge Point Operator:** a CPO is an organization responsible for managing and maintaining networks of EV charging stations[3] [4].

In order to facilitate seamless communication and interoperability between EV and EVSE, it is crucial to have a communication controller present on both ends. With numerous charging modes and standards, with different communication interfaces, this project endeavors to create and simulate the necessary hardware schematic for developing a Supply Equipment Communication Controller (SECC) conforming to the CCS standard, which will be further discussed in this document.

[1] Unlike conventional vehicles fueled by gasoline or diesel, EVs produce zero tailpipe emissions, making them an environmentally friendly alternative.

[2] EVSE facilitates the convenient and efficient charging of EV batteries, supporting the widespread adoption of electric vehicles. Charging stations can be installed in various locations, including homes, workplaces, public parking areas, and along highways, providing EV owners with the flexibility to recharge their vehicles wherever they go.

[3] CPOs ensure the availability, functionality, and reliability of charging infrastructure for electric vehicle users. They handle tasks such as station installation, maintenance, billing, and customer support. By collaborating with stakeholders such as governments, utilities, property owners, and EV manufacturers, CPOs play a crucial role in expanding and optimizing the EV charging network, ultimately facilitating the transition to sustainable transportation.

1.2 Problem Identification and Objectives

i-charging faces a significant challenge in the dynamic electric mobility sector, which is relying on external manufacturers for crucial devices, such as the Supply Equipment Communication Controller (SECC). The unpredictable nature of the stock market and other global conjunctures can impact supply chains and stock availability, leading to potential delays or disruption in production schedules. Moreover, price fluctuations from external suppliers can cause budgetary uncertainties, affecting profitability. Furthermore, relying on external suppliers often compromises specifications, limiting i-charging ability to customize products according to specific specifications. This limitation can have an adverse effect on competitiveness and market differentiation.

Therefore, from the company perspective, there has been a growing desire to design its own SECC. The primary objectives have been to achieve:

- **Self-sufficiency:** develop an in-house SECC solution to reduce dependency on external suppliers, ensuring stock availability stability and minimizing disruptions caused by market fluctuations;
- **Price Stability:** internalize production processes to mitigate risks associated with price fluctuations from external suppliers, providing greater control over costs and budgetary forecasts;
- **Enhanced Specifications:** create a customized SECC tailored to precise specifications, offering flexibility and adaptability to meet specific user needs;
- **Reliability and Quality:** ensure consistent product quality by internalizing manufacturing processes, reducing the likelihood of quality inconsistencies and delays caused by external suppliers;
- **Market Positioning:** in future scenario, i-charging can enhance its position in the electric mobility industry by providing SECC solutions that are of top-notch quality and can be customized according to specific user needs. These solutions should have superior specifications, which will help reinforcing the company status as a reliable and innovative industry player. Furthermore, offering such solutions will result in higher customer satisfaction levels, further boosting the company reputation.

The objective of this project is to meet the goals of the organization and initiate the first stage of the SECC project, which involves hardware development, encompassing:

- **Standards study:** analysing IEC 61851-1, IEC 61851-23, DIN 70121, and ISO 15118-3 standards to comprehend the technical requirements and functionalities necessary for the communication controller compliance;

- **Market analysis and existing solutions identification:** in-depth research of the current market of CCS communication controllers and identification of the State Of The Art (SOTA) solutions, technologies and industry trends;
- **Key components selection:** careful selection of Power-line Communication (PLC) chip, Microcontroller Unit (MCU), and other necessary components based on the analysis of the standards and market solutions, and detailed explanation of why these components were chosen, considering criteria such as performance, efficiency, compatibility and cost;
- **Circuit Design:** design of a detailed circuit schematic, incorporating all the necessary components and ensuring compliance with the internal requirements as long as the external ones established by IEC 61851, ISO 15118 and DIN SPEC 70121;
- **Test and validation of crucial circuit blocks:** by utilizing an electric circuit simulation software, various simulations can be performed with the aim of generating waveforms that depict specific points of the circuit. These waveforms can then be studied in order to better understand the behavior of the circuit and compare the results with expected outcomes. For instance, the rising and falling times of the voltage level, as dictated by a specific standard, can be analyzed using this method.

1.3 System Specifications and High-level Architecture

The following section presents the project specifications (both internal and standardized) and the system high-level architecture.

System Specifications

The project encompasses a total of 71 specifications (Figure 1.3). Out of these, 43 specifications are standard industry specifications adopted from IEC 61851, ISO 15118, and SAE J1772, which will be later presented in this document. The remaining 28 specifications are internal company specifications, which are mostly based on established standards. For instance, the SECC input voltage is set at 24 V to match the charger internal voltage supply. Some of these internal specifications were formulated through careful market research and comparative analysis.

This comprehensive approach ensures that the developed system not only meets the rigorous industry standards but also aligns with the company internal benchmarks, thereby contributing to a robust and clearly defined framework.

For further insight and details, please refer to Appendix A, which contains a table with all project specifications.

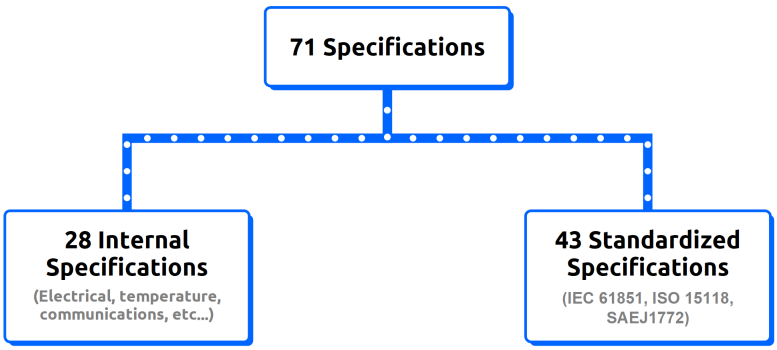


Figure 1.3: Project specifications nature

High-level Architecture

Figure 1.4 ilustrates the system high-level architecture, wherein the light-blue block represents the SECC. This architecture displays the general surroundings that are common to a SECC that complies with CCS. Any charging process intervenients that interact and communicate directly with the SECC during an actual charging process are external blocks depicted outside the light-blue box in the figure. The architecture consists of primary components and the communication interface Serial Peripheral Interface (SPI) that is chosen between the PLC chip and the MCU.

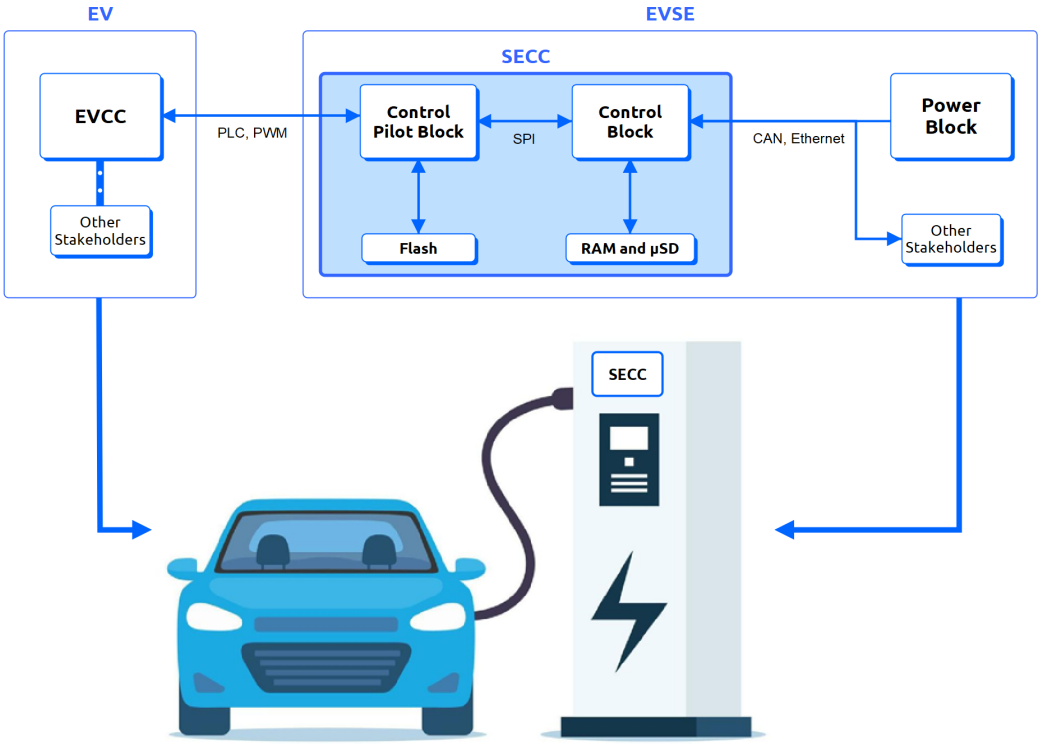


Figure 1.4: System High-level architecture - the blue box is the focus of this Thesis

As previously explained, the SECC plays a significant role in the communication between the (EV) and the EVSE, and it makes part of the EVSE, as shown in Figure 1.4. According to the IEC 61851 and ISO 15118 standards, which are addressed in sub-subsection 2.1.3, the communication interface between the Electric Vehicle Communication Controller (EVCC) and the Supply Equipment Communication Controller (SECC) must be Power-line Communication (PLC) for high-level communication and PWM signal for low-level, as displayed in Figure 1.4. The interface for communication between the *Power Block* and the SECC within the EVSE is not standard. However, this project specifications have defined CAN and Ethernet as the communication interface between the two blocks.

It is noteworthy to mention that while there exist multiple ways to implement the SECC, a generic implementation has been presented in order to facilitate the readers' comprehension of the subject matter. These building blocks represent a crucial aspect of practical implementation, thereby providing a contextual framework for the operational functionality of SECC in real-life scenarios. Please find below the definition/purpose for each of these building blocks:

- **EVCC:** it is the communication controller on EV side;
- **Power Block:** it is responsible for managing all power control and supply for the EV, including controlling the current and voltage levels and answering to emergency stop triggers on the EVSE side, among other functions;
- **Control pilot block:** this block is responsible for the communication interface between the EV and EVSE; it generates and receives high and low-level signals via the PLC and PWM interfaces; this block is equipped with a System on a Chip (SoC), as well as various filter circuits and drivers;
- **Control Block:** this block is representative of the core of the SECC, containing the MCU, essential communication interfaces, and peripherals that are crucial for the SECC to operate at its optimum level;
- **Other Stakeholders:** supplementary components or devices that are required for the charger to function properly; these may include sensors or the *Human Machine Interface* (HMI) controller.

1.4 Research Approach

This section outlines the research & development approach adopted for the project, encompassing project management, planning strategies, as well as the techniques and tools utilized throughout.

Milestones and timeline

The project Gantt chart, created on the freeware ProjectLibre, provides a visual representation of the project schedule. Figure 1.5 displays a collapsed version, offering a high-level overview of the project schedule with minimal detail, allowing for a comprehensive understanding of the project's timeline. The complete Gantt diagram is provided in Appendix B, where the parent tasks are expanded, unveiling the smaller tasks, emphasizing how larger tasks are segmented into smaller, more manageable subtasks. This breakdown enhances predictability and facilitates better control over work organization and scheduling.

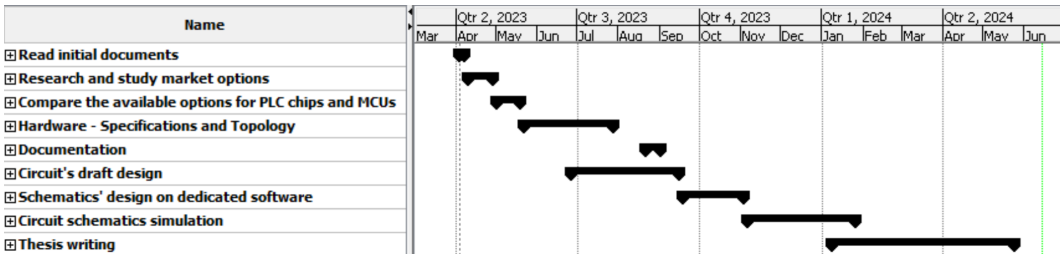


Figure 1.5: General Gantt chart (ProjectLibre)

Project Management

Azure DevOps [5] (Microsoft), is an all-inclusive suite of development tools that integrates various functionalities, including version control, automated testing, continuous integration, and deployment. It helps teams to collaborate more effectively and to manage the software development lifecycle efficiently.

Scrum [6] is an agile project management framework that emphasizes adaptive planning and iterative development. It breaks down projects into sprints, which are short, manageable iterations in which teams work together to deliver incremental value. Daily stand-up meetings and weekly sprint sessions help teams prioritize tasks and maintain alignment to meet customer needs and business objectives.

At i-charging, the Scrum methodology is implemented in the Azure DevOps Boards interface to optimize workflow processes. Integrating these methodologies cultivates a culture of innovation, continuous improvement, and efficient work and team management.

Features such as *Boards*, *Backlogs*, and *Sprints* are used within Azure DevOps to support Scrum practices. Boards provide a visual representation of work items, allowing teams to track progress and prioritize tasks easily. Backlogs help teams managing product requirements and planing future work, while Sprints facilitate the execution of short, time-boxed iterations.

Figure 1.6 shows an example of two project tasks added to the *Hardware Topology* Backlog, which is a part of the Feature known as SECC. The state of a task may

differ, such as being in *Testing* or currently *In progress*. Status are updated during daily or weekly meetings. Additionally, new tasks are added every sprint, which occurs every two weeks at i-charging.

Work Item Type	Title	State	Priority	Iteration Level 2
Feature	SECC	New	2	Sprint 48
Product Backlo...	Review of State of Art	Done	2	Sprint 38
Product Backlo...	HW topology	Done	2	Sprint 48
Task	Diagrama de blocos sistema	Done	2	Sprint 35
Task	Lista circuitos necessários	Done	2	Sprint 38

Figure 1.6: Scrum practices within Azure DevOps Boards interface - example for this project

Moreover, Azure DevOps offers reporting and analytics capabilities, enabling teams to monitor performance and identify areas for improvement throughout the project lifecycle.

1.5 Contributions

The pipeline block diagram in Figure 1.7, showcases the contributions in this Thesis. The objective is to provide a clear understanding of the author's work and highlight the various stages of the project that other members of i-charging supported.

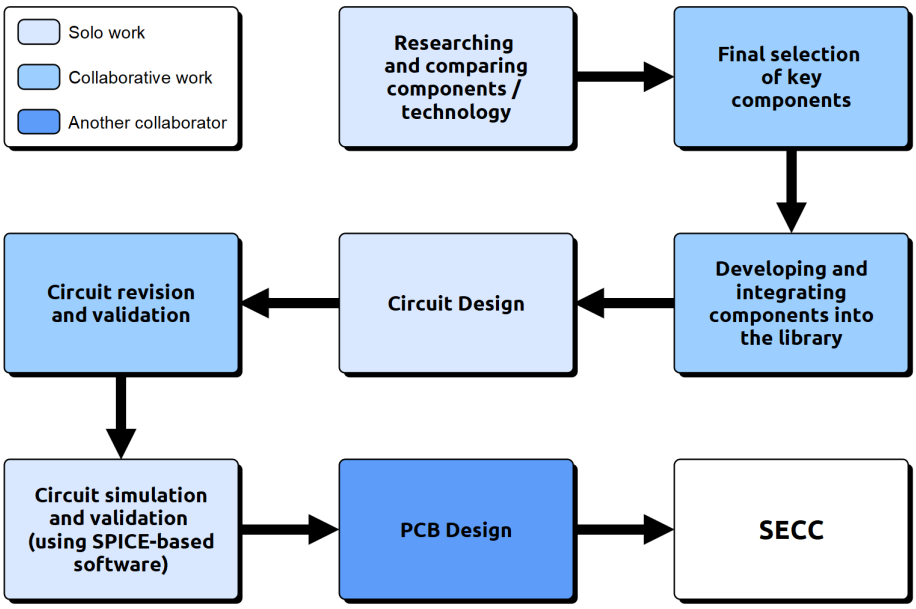


Figure 1.7: Project contributions pipeline diagram

The blocks colored in lighter blue represent the author's independent research and development efforts, as explained in the legend. Middle blue blocks denote

collaborative work. Darker blue blocks indicate work from other team members. The PCB design work is still pending, but it is expected to commence shortly, to be able to achieve the ultimate objective of this project, which is producing a CCS compliant SECC printed circuit prototype.

1.6 Document Structure

The remainder of this project is organized as follows:

The 2^{nd} Chapter starts with a market analysis, namely of SECCs technology. The third and fourth section discusses relevant technological background. The selection of key components and simulation tool for this project resulted from an exhaustive comparison and analysis reflected in these subsections.

The 3^{rd} Chapter presents the implementation of the circuit schematics, which are thoroughly explained, along with the rationale behind their design. The intention is to provide a comprehensive understanding of the circuit blocks and their role in the overall system.

The 4^{th} Chapter outlines the system debugging, evaluation and testing. These three stages are carried out not only with specialized software tools for debugging and simulation but also with human analysis for evaluation and validation. The conclusions and results of these crucial stages are presented in this chapter.

The final Chapter summarizes the overall conclusions, potential outcomes, and future work.

Chapter 2

Technological Context and Selection

This chapter offers a comprehensive examination of the technology landscape surrounding Electric Vehicle supply equipment (EVSE). It covers the full range of charging modes and standards currently in use, along with a detailed exploration of the purpose and technological context of a SECC. Commercial-off-the-shelf controllers with comparable features and specifications are also presented. Furthermore, an in-depth analysis and comparison is included to support the design options, such as the selection of the MCU and circuit simulator.

2.1 EV Charging

This introductory section provides an overview of the current charging technology, charging modes, and the different standards that govern them. Additionally, it explains the role of a communication controller and the compliance requirements it must meet to ensure efficient and reliable operation for the EVSE and user.

2.1.1 Charging Modes

As per the International Electrotechnical Commission (IEC) standard IEC 61851-1 [7], titled "Electric vehicle conductive charging system – Part 1: General requirements", there exist four different charging modes. Figure 2.1 illustrates the primary

distinctions between them, with the two most important factors being the presence or absence of control and communication and the amount of power supplied in a given time interval, which determines the speed of the charging process.

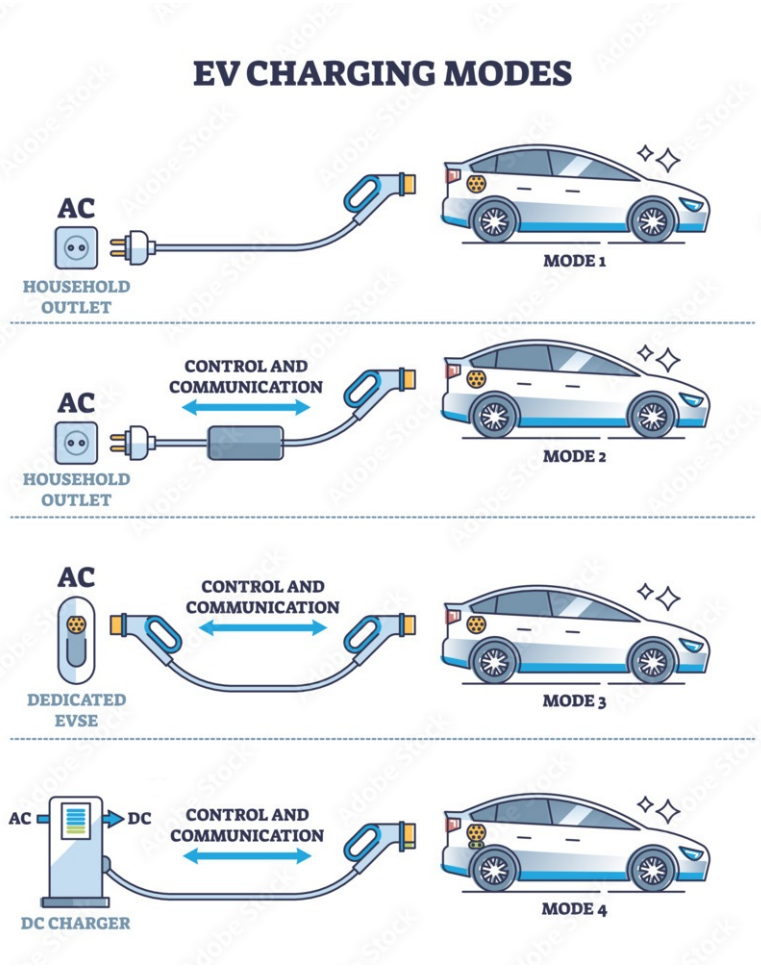


Figure 2.1: Electric vehicle charging modes [8]

This project aims at developing a SECC for controlling the Direct Current (DC) charging process of an EV with CCS (presented in the following subsection), as Mode 4 in Figure 2.1.

A DC fast charger for electric vehicles is a high-power charging station that delivers DC power to rapidly recharge EV batteries. Unlike slower Alternating Current (AC) chargers, DC fast chargers can significantly reduce charging times, making them ideal for long-distance travel and high-demand charging scenarios.

Briefly, a DC fast charger is made up of filters, rectifiers, and DC/DC converters, as the blocks shown in Figure 2.2.

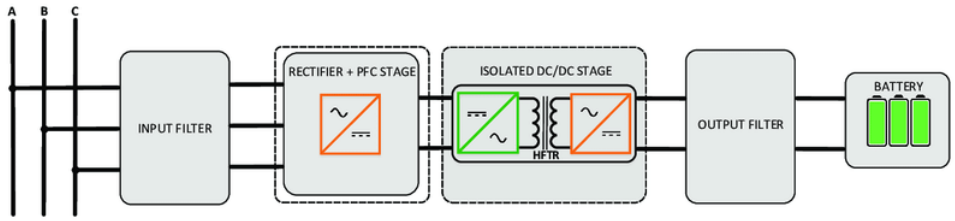


Figure 2.2: Basic blocks of DC fast charger power stage [9]

2.1.2 Charging Standards

There are both AC and DC charging methods, with the latter commonly referred to as fast charging. Various charging and safety standards were published worldwide, leading to the development of different charging standards and the respective official connectors with different characteristics and specifications. These connectors and standards resulted from the collaborative efforts and decisions of various commissions and associations worldwide. The different connectors are presented in Figure 2.3.

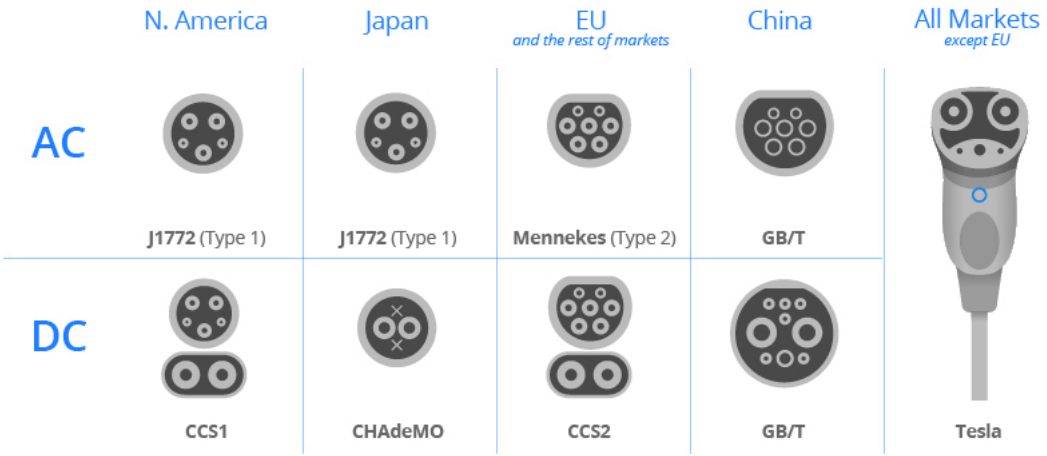


Figure 2.3: Different charging protocol plugs produced and used across the globe [10]

From Figure 2.3, it is evident that the connectors used in electric vehicles have different layouts, state signal pins, formats, and charging standards. This leads to diverse output power levels (for the EV), communication interfaces between the EVSE and the EV, and implementations. The *J1772* connector (Type 1) supports single-phase AC charging for Level 1[1] and Level 2[2] chargers, while *Mennekes* (named after the company that designed it, also known as Type 2) supports single-phase and

[1]Level 1 charging uses a standard 120 V household outlet and is the slowest option, taking up to 20 hours for a full charge (in countries with a main supply of 120 V) [11]

[2]Level 2 charging is faster, using a 240 V outlet and charging in 4-8 hours in Europe and other regions [11]

three-phase for Level 2 chargers [12]. *GB/T* protocol will not be discussed here as it is irrelevant to this project.

The *Combined Charging System* standard and respective connector, developed by a consortium of well-known automakers, allows both AC and DC charging with the same inlet. The implementation of DC charging is intended to deliver more power in less time. The CCS type 2 connector uses only two signal pins, one earth ground pin for communication, and two power cables for DC charging (Figure 2.4, below). Alternatively, the Mennekes plug (Figure 2.4, below) can be connected to the same CCS type 2 socket inlet illustrated in Figure 2.3 in order to provide AC charging. Therefore, the standard was named *Combined Charging System* due to the combination of power DC pins with the existing Mennekes connector.

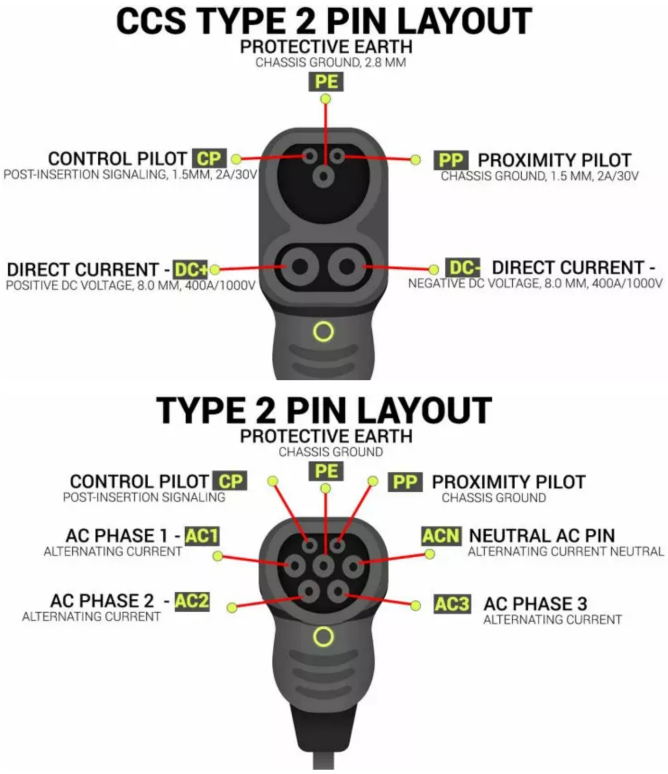


Figure 2.4: CCS type 2 and Mennekes (Type 2) plugs pinout [13]

Although *CHArge de MOve* (CHAdeMO) was the first DC charging standard to be introduced and rapidly adopted in Europe, CCS Type 2 quickly took over the European Union (EU) market once it was launched. All European automobile brands have now adopted the CCS Type 2 once it supports more output power and it combines AC and DC charging in a single inlet. Contrarily, CHArge de MOve (CHAdeMO) does not offer this feature [14].

When discussing CCS, it is important to mention the *Tesla* connector, which can be used for both AC and DC charging worldwide except for the EU. In order to expand sales to the European market, Tesla manufactured the Model S and X with

a Mennekes modified socket outlet (Figure 2.5), enabling Tesla users in Europe to charge their vehicles in any available AC charger [15]. However, DC charging is only possible in specific modified Tesla fast charging stations, or by utilizing adapters. These charging points used the Mennekes Plug, which was modified to allow for DC charging. In this case, the four pins that were used for AC charging were shunted on two pairs for the positive and negative sides of the DC charging.

Figure 2.5: Tesla socket inlet modified for Mennekes plug [16]

Later, in 2019, Tesla allowed its European customers to use any available DC fast charger by incorporating CCS Type 2 connectors in its Model 3 and Y vehicles. This move has cemented the CCS standard as the dominant charging connector in Europe. Although it is recommended for newly produced cars to feature CCS, many older vehicles still make use of the CHAdeMO connector. As a result, almost every DC charger in Europe has one CCS connector output (at least one is required for each fast DC charger) and one CHAdeMO connector output.

It should be noted that the history of CCS type 1 and CHAdeMO is identical for non-Tesla EVs in both United States of America (USA) and EU. However, in 2022, Tesla replaced its proprietary charging connector (also known as the Tesla connector) with a new charging standard called *North American Charging Standard* (NACS). Furthermore, Tesla made the specifications of this new standard available to other EV manufacturers. Unlike the Tesla proprietary connector, which communicates using *Controller Area Network* (CAN) bus, NACS uses Power-line Communication (PLC) just like CCS. Furthermore, it is worth noting that the North American Charging Standard (NACS) and CCS systems conform to the same ISO 15118 and IEC 61851 standards (which will be presented later in this section, as well as the DIN 70121). This means that any CCS-compliant EV has the same communication controller interface with the EVSE as NACS EVs have. It is then expected that in the upcoming years, the NACS connector and standard will become more popular than the CCS type 1 and CHAdeMO in USA [17].

This context is essential for showcasing the importance and global reach of the CCS standard. It is especially relevant to this project because every charger output that conforms to the ISO 15118, DIN 70121, and IEC 61851 standards for electric vehicle and electric vehicle supply equipment high-level and low-level communication, which includes CCS type 1, type 2 and NACS, necessitates a SECC. The subsequent subsection will describe the function of a SECC.

2.1.3 Supply Equipment Communication Controller (SEEC)

The *Combined Charging System* (CCS) is a pivotal component in the electric vehicle charging infrastructure (Figure 1.4). This controller is meticulously designed to facilitate seamless and efficient charging processes, tailored specifically to support a range of charging protocols and standards. This entails the establishment of robust connections with the vehicle's onboard systems, negotiation of crucial charging parameters such as voltage and current levels, and vigilant monitoring of the charging session to ensure safety and optimal performance. While this project acknowledges the existence and potential utilization of various standards and charging modes, such as CHAdeMO and AC charging, the project main focus is developing a SECC hardware that supports CCS.

Therefore, the EV communication controller core functionality revolves around its ability to interface with CCS-equipped electric vehicles, enabling a smooth communication and coordination during the charging process. In order to establish that communication interface, the SECC needs to adhere to specific parts of the ISO 15118 and/or DIN SPEC 70121 standards, along with the IEC 61851 standard, which will be briefly introduced.

IEC 61851

The IEC 61851 standard outlines the specifications for EV conductive charging systems. It covers the characteristics and operating conditions of the EV supply equipment, as well as the requirements for the low-level communication between the EV and the EVSE. This standard also includes specifications for electrical safety for the EV supply equipment.

ISO 15118

ISO 15118 is an international standard that provides guidelines for the high-level communication interface between EVSEs and EVs. It applies to all types of charging, including AC, DC, wireless, and pantograph. The standard specifies certain sections that outline the communication protocol to be adhered to during the charging process [18].

It is crucial to emphasize that adopting *HomePlug Green PHY* (HPGP) standard is mandatory by ISO 15118-3, delineating the necessary network and application protocol specifications. As highlighted earlier in this document, the CCS charging standard designates PLC as the communication interface between EVs and EVSEs. Consequently, the specified powerline standard within the CCS framework is unequivocally *HomePlug Green PHY*.

DIN SPEC 70121

DIN SPEC 70121 is a standard similar to ISO 15118, which defines the communication interface between a DC charging station and an EV. It outlines the protocols and procedures that must be adhered to during the DC charging mode. However, it is less comprehensive than ISO 15118, which provides standards for both AC and DC charging modes, thus covering a wider range of charging scenarios.

This German standard was instituted prior to ISO 15118 and is endowed with fewer features. It does not incorporate specific functionalities such as plug&charge and smart charging, which are present in ISO 15118 [19]. Nevertheless, DIN SPEC 70121 and ISO 15118 share the same objective and foundation, and their communication interface standards are identical.

It is possible that certain EV meet only DIN SPEC 70121, some only meet ISO 15118, and others meet both of them. This same situation can also occur with the supply equipment. When there are multiple compatible options available, the EV communication controller must select which standard to adhere to.

In summary, the SECC is a crucial component in the EVSE. From the point of view of this project, it has to be tailored to support the CCS protocol and ensure seamless communication and coordination with CCS equipped electric vehicles, adhering to standards such as IEC 61851, ISO 15118, and DIN SPEC 70121.

2.2 Commercial off-the-shelf SECCs

In this section, a comprehensive analysis of the SECCs available in the market is presented. The purpose of this analysis is to gather publicly available information on various controllers, with the aim of discerning and comprehending the key features of each controller. By doing so, it is possible to gain a better understanding of their potential applications and limitations.

2.2.1 EVAcharge SE

EVAcharge SE [20] (Figure 2.6) is a communication controller fully compliant with CCS standards, conforming to both DIN 70121 and ISO 15118 specifications, and establishing communication for one EVSE output. EVAcharge SE does not have a

pre-installed software stack. This device streamlines communication between EVSE and EV. It seamlessly integrates with EVs that also adhere to ISO 15118 / DIN 70121 standards, and allows the charge controller to establish communication with the EV. The platform supports both CP and Proximity Pilot (PP) signaling, as well as *HomePlug Green PHY*.

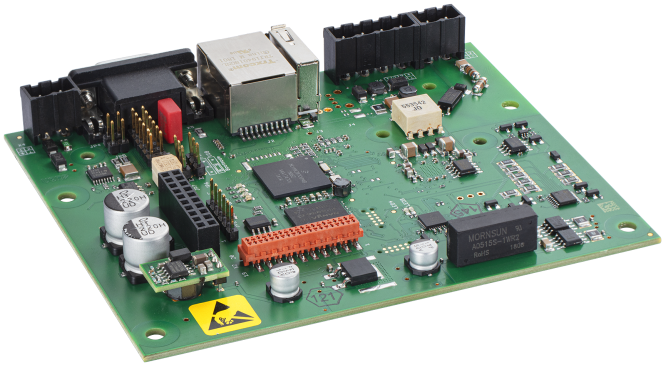


Figure 2.6: EVAcharge SE, a product offered by Chargebyte SECC. [20]

2.2.2 vSECC

The vSECC, showcased in Figure 2.7, is an interface product from Vector that streamlines communication for electric vehicle charging across multiple standards like CCS, NACS, CHAdeMO, and Pantographs. Specifically designed to meet the requirements of public or semi-public fast charging stations, this SECC can manage up to two charging outputs. Additionally, public charging point operators can avail of authorization options like Plug & Charge. Vector has also developed the communication interface for high-level communication, which is integrated into the vSECC software [21].

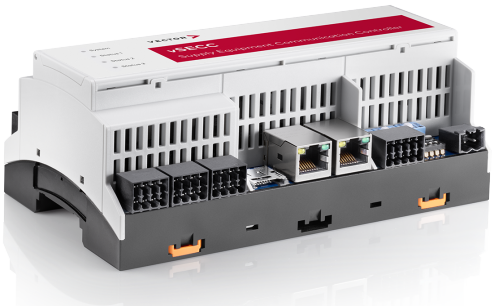


Figure 2.7: vSECC, a product offered by Vector [21]

2.2.3 Peppermint

PEPPERMINT, a certified CCS solution developed by Gridwiz (Figure 2.8), is a PLC based modem designed for DC charging, adhering to ISO 15118, DIN 70121, and IEC 61851 communication standards. This modem processes HPGP communication standard essential for CCS EV charging while also supporting RS232, RS485, and CAN interface for other communication standards between EVs and EVSEs. Equipped with a debug port for status monitoring, status LED, input-output port, and Ethernet port for external service connectivity, PEPPERMINT can be integrated into chargers using DIN-rail (EN 50022) mounts or wall-mount brackets, offering a diverse, scalable, and convenient connection between EVs and EVSEs. Its stability is ensured through a certified software stack. Additionally, it is designed with Vehicle-to-Grid scalability, enabling support for Value Added Services (VAS) and External Identification Means (EIM) via the Ethernet port [22].

Figure 2.8: Peppermint, a product offered by Gridwiz [22]

2.2.4 Synthesis and Reflections

Among the Commercial-off-the-shelf (COTS) SECCs adressed, the latest three embody the essential features that any dependable SECC should have. Table 2.1 identifies the most significant available online features that the three SECCs possess.

Table 2.1: Comparative table of the most important SECC features

Parameter \ SECC	EVAcharge SE	vSECC	Peppermint
Processor	NXP i.MX287	NXP i.MX 6Quad Core	ARM Cortex-A8 800 MHz
PLC Chip	Qualcomm QCA7000	-	-
Storage Flash	4 GB	8 GB	-
Storage RAM	128 MB	2 GB	1 GB
Operating System	Linux	-	Linux
Temperature Range	- 40 °C to +85 °C	- 40 °C to +70 °C	- 40 °C to +85 °C
Interfaces	Ethernet, CAN, USB	Ethernet, CAN, USB	Ethernet, CAN

By analyzing and comparing the characteristics presented above, it becomes feasible to identify the necessary attributes that a CCS communication controller must have. These include:

- **High-performance Processor:** must feature at least one Arm Cortex-A8 (the oldest Cortex-A processor in the market) with dual 32-bit cores, operating at frequencies ranging from 300 MHz up to 1.2 GHz;
- **HPGP SoC:** Compliance with ISO 15118 / DIN 70121 standards;
- **PWM Generator:** Must adhere to IEC 61851-1 standards;
- **High-storage Interface Capacity:** 500 Mb to 1Gb DDR Memory;
- **Temperature Range:** Industrial Grade (-40 °C to +85 °C);
- **Operating System:** Must be Linux compatible;
- **External Interfaces**: At least Ethernet, CAN and USB.

The careful evaluation and selection of the most appropriate MCU and HPGP SoCs is crucial due to the importance of their primary features just presented. The following section outlines some relevant options for both MCU and HPGP SoCs and provides a thorough analysis and justification for the system options. It is important to note that other features, such as cryptography (which is specified in the project specifications), will also be taken into consideration during the following analysis.

2.3 MCU and PLC Chip

This section entails a comprehensive analysis, comparison, and selection of the primary SoCs of the system. The main objective is to choose the most appropriate, comprehensive, and high-performance chips. The evaluation will consider several factors, including but not limited to the technical specifications, processing power, energy efficiency, and cost-effectiveness of the two options. After a thorough examination of the pros and cons of each SoC, a final decision will be made based on the merits of the most suitable chips according to the project's specifications.

2.3.1 Microcontroller Unit

The initial selection process involves meticulously evaluating a pool of MCUs, with a strong emphasis on identifying the key characteristics that a SECC MCU must possess, as outlined in the previous section. Hence, the candidate MCUs are as follows:

- **STM32MP153F [23]:** the STMicroelectronics MCU featuring a dual-core Arm Cortex-A7 running at 800 MHz, along with an Arm Cortex-M4 real-time coprocessor, FD-CAN, secure boot capabilities, and cryptography support;
- **AM3352 [24]:** the Texas Instruments Sitara processor equipped with an Arm Cortex-A8 core, 1 GB Ethernet, display functionalities, and CAN compatibility;
- **i.MX 6ULL [25]:** the NXP Single-Core Processor featuring an Arm Cortex-A7 core;
- **ST2100 [26]:** the STMicroelectronics broadband powerline communication SoC.

All of the SoC packages that will be discussed in the forthcoming feature analyses and comparisons are BGAs packages. A generic example of a *Ball Grid Array* (BGA) package is depicted in Figure 2.9.

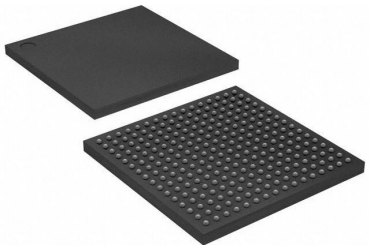


Figure 2.9: Generic BGA package [27]

Note that the ST2100 was considered in this analysis due to its generic compliance with all the specified criteria, including its support for the HPGP standard [26], a significant project specification. However, as will be evident from the upcoming analysis, it exhibits slightly reduced features and performance.

The following table presents a succinct comparison of the key features that are vital to be present on the microcontroller as per the project specifications. A more comprehensive comparative table is presented in Appendix C, Section C.1. Please note that the latter table includes additional information that may be useful for a more in-depth analysis of their features. Please also note the Table 2.2 legend and take into consideration the Appendix C - Section C.1 text color for each feature.

Table 2.2: MCUs comparative table

Parameter \ Part Number	STM32MP153F	AM3352	i.MX 6ULL	ST2100
Main processor				
Co-processor				
External Memory Interfaces				
On chip memory				
Cryptography				
Conectivity				
Power modes				
ADC				
Clocks				
Timers				
Availability				
Price and mimimum quantity				
Development kit				
Suport				

Ideal (free/cheap, better, more complete)
Limited (acceptable, basic features)
Insufficient (small, non-existent, expensive)

The color green indicates an ideal feature, while yellow and red represent limited and insufficient, respectively. This classification system allows for a visual comparation of the presented MCUs, providing a clear indication of the most suitable option. For ease of understanding, conclusions have been drawn (based on the information presented in Appendix C - Section C.1) for each feature:

- **Main Processor:** the STM32MP153F, AM3352, i.MX 6ULL and ST2100 CPUs share similarities in their 32-bit Reduced Instruction Set Computing (RISC) architectures, characterized by streamlined instruction sets designed for faster execution. The STM32MP153F employs a dual-core ARM Cortex-A7 architecture running at up to 800 MHz, featuring 32-bit processing and 32 KB instruction and data caches per core. Similarly, the AM3352 and i.MX 6ULL adopts single-core ARM Cortex-A8 and Cortex-A7 architectures, respectively, clocked at up to 1 GHz and 900 MHz, with comparable cache configurations. ST2100, when compared to the other options, has a lower cache memory and significantly lower core operating velocity. As such, it is evident that the core processors of STM32MP153F, AM3352, i.MX 6ULL and ST2100, are the most suitable options. However, the STM32MP153F holds a brief advantage due to its dual-core processor;

- **Co-processor:** the STM32MP153F features an ARM Cortex-M4 co-processor alongside its dual-core Cortex-A7, enabling efficient handling of real-time tasks and low-power operation. Similarly, the i.MX 6ULL integrates a co-processor, typically a Cortex-M0+ or Cortex-M4 variant, enhancing its versatility for tasks like sensor interfacing and power efficiency optimization. These co-processors complement the main cores, allowing both chips to excel in various

embedded applications. Hence, upon comparison with the other two MCUs, these two exhibit an advantage with this feature;

- **External Memory Interface:** the STM32MP153F, AM3352, i.MX 6ULL and ST2100 processors share similar memory interfaces, supporting DDR-SDRAM, NAND/NOR Flash, and additional storage options like eMMC and SD card. However, the main difference lies in the STM32MP153F's 32-bit DDR-SDRAM interface, offering potentially higher memory throughput compared to the 16-bit interfaces of the other processors. This 32-bit capability can enhance data processing performance in certain applications, distinguishing the STM32MP153F in terms of memory bandwidth and efficiency;

- **On-chip Memory:** the STM32MP153F, AM3352, i.MX 6ULL and ST2100 MCUs boast similar on-chip memory features, including general-purpose RAM and boot ROM, tailored to their respective architectures. However, STM32 stands out with greater capacity in both RAM and ROM compared to the others;

- **Cryptography:** STM32MP153F, AM3352, i.MX 6ULL and ST2100 MCUs possess inherent cryptography capabilities that are essential for safeguarding sensitive data from potential future data-changing through the SECC between the EV and the Charge Point Operator (CPO). These features include encryption, decryption, secure key storage, and hashing algorithms, ensuring data confidentiality, integrity, and authenticity;

- **Conectivity:** the STM32MP153F, AM3352, i.MX 6ULL, and ST2100 microprocessors offer a range of communication interfaces suitable for diverse embedded applications. While all share similarities, the STM32MP153F stands out with a more extensive array of interfaces. However, the ST2100 lacks the SPI interface, which can be crucial for potential communication between the two SoCs;

- **Power Modes:** the STM32MP153F, AM3352, and i.MX 6ULL microprocessors offer similar power modes, allowing for efficient power management based on application requirements. These modes include options such as active, sleep, standby, and deep sleep modes, enabling the adjustment of power consumption levels based on processing needs. However, specific details regarding power modes for the ST2100 are not currently available online;

- **ADC:** the STM32MP153F Analog-to-Digital Converter (ADC) typically offer resolutions of up to 12 or 16 bits, providing precise measurements at mega samples per second (Msps) rates. In contrast, the AM3352 and i.MX 6ULL

usually provides ADC resolutions of up to 12 bits, with sampling rates ranging from tens to hundreds of kilo samples per second, significantly lower than the STM32MP153F. Unfortunately, specific technical specifications for the ST2100's ADCs are unavailable online;

- **Clocks:** the STM32MP153F, AM3352, i.MX 6ULL and ST2100 are equipped with integral clocking systems that are crucial to their functionality. However, they differ in terms of their clocking capabilities. The STM32MP153F offers a faster internal oscillator, namely the High-Speed Internal (HSI) oscillator, and supports larger external oscillators, which provide it with greater versatility in clocking options. On the other hand, while the clocking systems of AM3352, i.MX 6ULL, and ST2100 offer reliability and stability, they do not match the speed and flexibility of the STM32MP153F;

- **Timers:** the STM32MP153F microprocessor offers a broader variety of timers compared to the AM3352, i.MX 6ULL, and ST2100. It includes general-purpose timers, advanced-control timers, and watchdog timers, providing versatility for various timing requirements in embedded systems. These timers offer advanced features such as PWM, input capture, and output compare functionalities, enabling precise timing control and event generation. In contrast, while the AM3352, i.MX 6ULL, and ST2100 also provide timers suitable for general-purpose tasks, they may lack the advanced features and variety found in the STM32MP153F. These timers are essential for coordinating system activities and ensuring the proper operation of embedded applications;

- **Packages:** the STM32MP153F, AM3352, i.MX 6ULL, and ST2100 microprocessors are packaged in Ball Grid Array (BGA) packages, offering varying numbers of pitch balls and package sizes. This variation is primarily based on the processor's pin count and peripheral features. STM32MP153F and AM3352 often come in larger BGAs to accommodate extensive peripherals, while i.MX 6ULL and ST2100 may feature smaller packages due to simpler configurations. Nonetheless, all BGA packages ensure efficient heat dissipation and reliable electrical connections for diverse embedded applications;

- **Availability, Pricing, and Suppliers:** the STM32MP153F, AM3352, and i.MX 6ULL microprocessors are readily available from various suppliers, with no minimum order quantity required. These processors are typically in stock and accessible for purchase in quantities as small as one unit. While the STM32MP153F tends to be slightly more expensive than the AM3352 and i.MX 6ULL, the price difference is minimal. Samples can be readily obtained for these processors, making them suitable for initial prototype development stages where only a small quantity is needed, without immediate plans for

mass production. However, the ST2100 microprocessor is only available for purchase in quantities multiples of 1134, which may not be ideal for projects requiring small-scale development or prototyping;

- **Development Kit:** the STM32MP153F, AM3352, and i.MX 6ULL MCUs are supported by development board kits, essential for understanding MCU functionality and kickstarting project development. These kits provide platforms for experimentation and prototyping, including necessary components like power supplies and interfaces. With software development tools and examples, it's possible to start coding and testing applications before finalizing the SECC PCB design, making the development board an invaluable resource for learning and accelerating the project development;

- **Support:** manufacturers support for the STM32MP153F, AM3352, i.MX 6ULL and ST2100 microprocessors vary, with STMicroelectronics standing out for its robust support. Based on experience and feedback from resellers during project development, ST typically offers extensive documentation and readily accessible resources. It is worth noting that the availability of online documentation for the STM32MP153F and AM3352 is considerably vast in comparison to the manufacturers of the i.MX 6ULL, and ST2100, who may require a non-disclosure agreement (NDA) for accessing more detailed information. This disparity highlights the crucial consideration of manufacturer support when selecting a microprocessor for a project. The STM32MP153F, with its comprehensive support ecosystem, is preferred over its counterparts.

After the examination conducted in this sub-section, it can be concluded that the optimal MCU for this project is the **STM32MP153F**.

2.3.2 PLC Chip

The initial selection process involves meticulously evaluating a pool of PLC SoCs, with a strong emphasis on identifying the key characteristics that a SECC HPGP transceiver must have, as outlined in the previous section.

Hence, the selected PLC chips are as follows:

- **QCA7000/7005 [28]:** HomePlug Green PHY Single Chip Solution;

- **IS32CG5317 [29]:** an automotive grade, HPGP low power transceiver with SPI and ethernet interface designed for automotive applications;

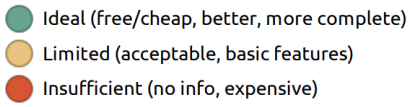
- **MSE1021 [30]:** high performance and integration SoC for high-Speed PLC applications.

It is important to note that the ST2100, which was considered as a potential 2-in-1 SoC for this project, was not included in this comparison. This decision was made because the ST2100 had already been eliminated in the MCU comparison phase, and it was not specifically developed for the EV interface, unlike the previously presented options.

Table 2.3 summarizes the key features that are vital to be present on the HPGP SoC as per the project specifications. A more comprehensive comparative table is presented in Appendix C, Section C.2. Please note that this table includes additional information that may be useful for a more in-depth analysis of the features.

Table 2.3: HPGP chips comparative table

Parameter \ Part Number	QCA7000/7005	IS32CG5317	MSE1021
Compliant with ISO 15118			
Operating temperature			
Conectivity			
Package			
Oscillator			
Boot			
Encryption			
External line driver			
PWM Generator			
Availability, pricing, and suppliers			
Support			



Please note the information presented in Table 2.3 legend, as well as the Appendix C - Section C.2 text color for each feature. The color green indicates an ideal feature, while yellow and red represent limited and insufficient, respectively. This classification system allows for a graphical representation of the presented HPGP SoCs, providing a clear indication of the most suitable option. For ease of understanding, conclusions have been drawn based on the information presented in Appendix C - Section C.2 for each feature:

- **Standards Compliance:** all presented SoCs are compliant with ISO 15118, DIN 70121, and HPGP. This ensures that the SoCs are equipped with an analog interface ready for receiving and transmitting data according to these standards;
- **Operating Temperature:** the three SoCs attend, at least, the industrial-grade standards for operating temperature (-40 °C to +85 °C), ensuring suitability for this project's requirements;

- **Conectivity:** each of the three SoCs features the same communication interface as specified in the project requirements, ensuring compatibility and interoperability across the system;
- **Package:** the QCA7000 is packaged in BGA, making it less prototype-friendly. Once soldered, the BGA is exposed to initial tests, and adding any extra provisional wiring on the chip becomes impractical with this package. On the other hand, the CG5317 and MSE1021 come in Quad Flat Package (QFP), offering an advantage in this comparative point as they allow for easier modification during prototype testing;
- **Oscillator:** all of the 3 SoCs feature a dedicated interface for an external single 25 MHz oscillator, ensuring precise and synchronized clock timing throughout the system;
- **Boot:** all three SoCs offer identical boot options, allowing booting from the host or external flash, providing flexibility in system initialization;
- **Encryption:** while MSE1021 and CG5317 feature encryption capabilities, information regarding encryption for QCA7000 is currently unavailable. Encryption is essential for safeguarding sensitive data and ensuring confidentiality, integrity, and overall system security;
- **External Line Driver:** while MSE1021 and CG5317 support an external line driver, details for QCA7000 are unavailable. An external line driver is vital for maintaining signal integrity and overcoming attenuation and noise issues, ensuring reliable communication over long distances and in noisy environments;
- **PWM Generator:** QCA7000 lacks available information regarding PWM generation, while CG5317 does not include this feature. However, MSE1021 offers an interface capable of generating PWM signals according to IEC 61851-1 standards for the control pilot circuit. Additionally, MSE1021 includes feedback pins that can read the signal it generates, allowing for real-time correction if necessary. This capability is essential in electric vehicle charging systems, ensuring precise control and monitoring of power transfer;
- **Availability, Pricing, and Suppliers:** CG5317 holds an advantage in availability and pricing, as it offers a lower price per unit compared to the others. However, all SoCs can be purchased individually, and samples may be available upon request. This flexibility ensures accessibility for various project needs;
- **Support:** MSE1021 holds a significant advantage in support, as confirmed through meetings and email exchanges with official manufacturers and distributors. MSE1021 offers comprehensive support for hardware and software development, including access to all documentation after signing a Non-Disclosure

Agreement (NDA). This level of support is crucial for developing and implementing custom software and firmware, making MSE1021 an optimal choice for the project. In contrast, support for software development with CG5317 requires purchasing Lumissil's evaluation board of the SoC. QCA7000 offers limited support, making the less favorable in this regard.

After a thorough examination of the color tables and analyses conducted in this sub-section, it can be concluded that the optimal HPGP SoC for this project is the **MSE1021** from VertexCom.

2.4 Circuit Simulator

While developing a prototype like the one under design, it is crucial to simulate the circuit to analyze its integrity and predict its behavior in a real-world environment. By using a simulator, it is possible to create waveforms by calculating specific values of voltage, current, and other parameters, at certain time intervals. This process allows the user to visualize how the circuit behaves under different conditions, helping to identify potential problems and make necessary improvements. The simulator calculates the values of the parameters based on the circuit design and the input signals provided by the user. This process allows the user to analyze the circuit response accurately and make informed decisions based on the results [31]. Therefore, choosing the appropriate simulator is essential to ensure the project effectiveness. To do so, it is crucial to understand the differences and specifications among the available simulators and select the one that meets the project specific needs.

2.4.1 Software Selection

This section will conduct a comparative analysis of some of the most commonly used electronic circuit simulators available in the market. It aims at evaluating their unique features, ease of use, simulation capabilities, and other essential factors.

The following simulators have been considered in this analysis:

- **SPICE [32]:** Simulation Program with Integrated Circuit Emphasis (SPICE) is a free computer program used by engineers to predict the behavior of electronic circuits through mathematical models. It was developed in the 1970s at the University of California, Berkeley, as a teaching tool for integrated circuit design. Throughout time, SPICE has undergone many changes, including the addition of new device models, enhancements in speed and capacity, and improvements in convergence for greater simulation precision [33]. These developments have allowed for the creation of multiple Simulation Program with Integrated Circuit Emphasis (SPICE) versions. It is important to note that none of these versions come equipped with a Graphical User Interface (GUI);

- **LTspice [31]:** it also is a free general-purpose software for simulating Electronical circuits based on SPICE, and it is the most widely used and distributed software worldwide. It was developed by Linear Technology, which is now part of Analog Devices, and, unlike SPICE, LTspice is not open-source and features a (GUI). One of the key differentiators of this SPICE-based software compared to SPICE itself is that, in addition to numerous pre-installed libraries of generic components in both software versions, LTspice users can benefit from numerous libraries developed by component manufacturers themselves;
- **ORCAD PSpice [34]:** two different software tools used to design and simulate Electronical circuits (based on SPICE). PSpice was originally developed by MicroSim Corporation and later acquired by Cadence Design Systems. PSpice is similar to the LTspice simulation interface, but it has the advantage of being integrated within Cadence Design Systems, which specializes in Electronic Design Automation (EDA), where every OrCAD tool takes place [35]. This integration makes it easier for users to develop and print Printed Circuit Boards (PCBs) as it establishes a seamless development path between circuit design and simulation. PSpice has a comprehensive and complex GUI, although it has a slightly less modern look;
- **Altium Designer Mixed Simulation [36]:** just like Cadence Design Systems, Altium Designer is an EDA company with an integrated simulation interface based on SPICE, called Mixed Simulation. It allows the use of models developed for specific software, such as PSpice and LTspice, and has a user-friendly GUI that is modern and comprehensive. However, the multitude of options available can make it a bit complex. The main difference between Altium and the other three software is that Altium has a cloud-based platform called Altium365.

It is worth noting that the last presented simulation software are SPICE-based, and as such, almost every analysis presented from here on will use SPICE models. However, there are other types of analysis that will not be carried out in this project but are as important to be done prior to prototyping the circuit. For instance, during the PCB design phase, it might be necessary to use different types of models to carry out signal integrity analysis, such as Input/Output Buffer Information Specification (IBIS) models. These are behavioral models that describe the analog behavior of the digital input and output buffers of a device. They consist of tabular data that explains the current-voltage (I-V) relationship of the components within the digital buffers, as well as the voltage across time (V-t) switching characteristics of the output or I/O buffers. Input/Output Buffer Information Specification (IBIS) models operate like black-box models, meaning they do not contain internal information that can be reverse-engineered [37].

2.4.2 Comparative Analysis

The following table (2.4) compares different circuit simulator software options in terms of their functionalities. Each column represents a separate software option, while the rows denote the specific features being compared. The comparison is shown through colored circles, where green indicates a positive attribute (such as being free, good, or user-friendly), yellow denotes a moderate attribute (such as having limited functionality or being moderately priced), and red signifies a negative attribute (such as being expensive, having no functionality, or being difficult to use).

Table 2.4: Electronic circuit simulators comparative table

Parameter / Software	Spice	LTspice	PSpice	MixedSim
Transient Analysis	🟢	🟢	🟢	🟢
AC and DC Sweep Analysis	🟢	🟢	🟢	🟢
Operating Point Analysis	🟢	🟢	🟢	🟢
Sensitivity Analysis	🟢	🟢	🟢	🟢
Parameter Sweep Analysis	🟢	🟢	🟢	🟢
Noise Analysis	🟡	🟢	🟢	🟢
Monte Carlo Analysis	🟡	🟢	🟢	🟢
Signal Integrity Analysis	🟡	🟡	🟢	🟢
Mixed-Signal Analysis	🟡	🟡	🟢	🟢
Temperature Sweep Analysis	🟢	🟢	🟢	🟢
Generic and Pre-installed Libraries	🟡	🟢	🟢	🟡
Add Third-Party Models	🔴	🟢	🟢	🟢
Create Simulation Model	🟢	🟢	🟢	🟢
Technical Support	🟡	🟡	🟢	🟢
Online Community	🟡	🟢	🟢	🟢
Learning Curve	🟡	🟢	🔴	🔴
Graphical User Interface	🔴	🟡	🟢	🟢
User-friendly Simulation Options	🔴	🟡	🟢	🟢
Integrated on EDA System	🔴	🔴	🟡	🟢
Online Work Based on Cloud	🔴	🔴	🔴	🟢
Licensing	🟢	🟢	🔴	🔴
Live Supplier Data	🔴	🔴	🔴	🟢
Manufacturers Encrypted Models	🟢	🟢	🟢	🔴

🟢 Yes (or free, good, soft)
🟡 Maybe (or limited, moderate)
🔴 No (or expensive, none, steep)

To make it clearer, the table parameters details are presented below, along with each respective description.

- **Transient Analysis [38]:** this is a type of simulation that calculates the circuit response over a specific period defined by the user. The accuracy of this analysis is dependent on the step size defined by the user. The step size determines the level of detail in the analysis. A low step size means more detail, and a big step size means less detail. The time step refers to the time interval between each calculation made by the simulation. By adjusting the time step

and the simulation time, the user can obtain a detailed understanding of the circuit's behavior over time;

- **AC and DC Sweep Analysis [39]:** the AC Sweep analysis calculates a circuit frequency response via small-signal AC output variables. It begins with an Operating Point analysis to identify DC bias, followed by analyzing the circuit over a frequency range using a sine wave generator. The output is typically a transfer function, like voltage gain or trans-impedance. This analysis is useful for optimizing circuit performance and identifying issues. The DC Sweep analysis produces an output similar to that of a curve tracer. It achieves this by conducting a series of operating point analyses that modify the values of specific parameters in predetermined steps to generate a DC transfer curve. This curve describes the relationship between the input and output of the circuit under different DC operating conditions;

- **Operating Point Analysis [39]:** this analysis is employed to identify the DC operating point of a circuit, with inductors replaced by short circuits and capacitors by open circuits. This analysis calculates the current and voltage balance points in a steady-state circuit operation, transfer coefficients in DC mode, and poles and zeros of the AC transfer characteristic. These results are essential in other types of calculations and provide a clearer understanding of the circuit's behavior during normal operation;

- **Sensitivity Analysis [39]:** this analysis is a powerful tool used to determine the components or factors that have the highest impact on a circuit's output characteristics. Identifying these elements helps minimizing negative effects or enhancing performance based on positive traits possible. Sensitivity Analysis calculates numeric values for given measurements related to circuit components or model parameters, as well as sensitivity to temperature and global parameters. The analysis results in a table of sensitivity values for each measurement type, providing a clear understanding of each component's impact on the circuit's performance;

- **Parameter Sweep Analysis [39]:** this feature modifies device, source, or temperature values in a defined range using specified increments. It is useful for analyzing circuit performance and identifying optimal parameter values. By visualizing the circuit response to different inputs, users can make informed decisions and optimize overall circuit performance;

- **Noise Analysis [39]:** The Noise analysis quantifies resistors' and semiconductors' noise contributions by plotting the Noise Spectral Density, measured in Volts squared per Hertz (V^2/Hz). Controlled sources, inductors, and capacitors are considered noise-free. This technique is useful for identifying and

mitigating noise sources in the circuit, allowing for optimal performance and reduced noise interference;

- **Monte Carlo Analysis [39]:** this analysis enables the user to perform multiple simulation runs with component values randomly varied across specified tolerance ranges. This technique is useful for identifying the statistical distribution of the circuit's output characteristics, enabling the user to optimize circuit design to account for component variability. By simulating numerous runs across the defined tolerance ranges, users can visualize the circuit performance under different scenarios (including worst-case scenarios), providing valuable insights into the circuit behavior and performance;

- **Signal Integrity Analysis [40]:** this analysis aims to implement different techniques in the process of PCB layout and routing in order to confirm that the signal remains intact while it travels from its origin to its end-point. However, it is important to note that digital signals are essentially analog in nature and are susceptible to several factors, such as distortion, noise, and loss. Therefore, signal integrity is essential to ensure that the digital signal transmitted between two points remains accurate and reliable. In this type of simulation, IBIS models are commonly used;

- **Mixed-Signal Analysis:** it is a comprehensive process that involves simulating and analyzing electronic systems that consist of both analog and digital components;

- **Temperature Sweep Analysis [39]:** this analysis allows users to simulate circuits at different temperatures within a specified range, generating a series of curves for each temperature setting. It can work in conjunction with other analyses and produce ten different waveforms for the same transient analysis with ten different ambient temperatures, for instance;

- **Generic and Pre-installed:** these are the generic component variety and quantity of manufacturers' components already present on pre-installed libraries;

- **Add Third-Party Models [41]:** there are various third-party models available from manufacturers that can be added to circuit simulations. Many device manufacturers provide SPICE models that correspond to the devices they manufacture. Typically, adding these models to a schematic component requires downloading the required model file and connecting it to the component;

- **Create Simulation Model [42]:** some SPICE models may need to be written from scratch, using hierarchical sub-circuit syntax to create the required sub-circuit model file (*.ckt). Manufacturers and suppliers may provide some

models as downloadable text files or present the model details as text on a browser page. In such cases, users can create a new model file and copy/paste the content from the browser page into it;

- **Technical Support:** the software support for technical doubts or problems;
- **Online Community:** the quantity, quality, and still active web forums about each software;
- **Learning curve [43]:** it is a mathematical representation that shows how a process can be enhanced over time with increased proficiency and learning;
- **Graphical User Interface:** also known as GUI, it is a type of user interface that uses graphical elements such as icons, buttons, and menus to help users interact with electronic devices;
- **User-friendly Simulation Options:** how interactive and organized are the GUI simulation options;
- **Integrated on EDA System:** if the software is integrated inside an Electronic Design Automation (EDA);
- **Online Work Based on Cloud [44]:** a cloud-based platform that enables electronic product design, real-time team collaboration, and data management, among other functionalities;
- **Licensing:** if user licensing is required, and what is the cost, that will vary depending on the specific product and the number of licenses needed;
- **Live Supplier Data:** design components linked to real-world parts, allowing the user to easily access real live data regarding the component, such as its price, availability in stock, and vendors who supply it;
- **Vendors Encrypted Models:** if vendors have specific encrypted models for the software.

Upon examination of the results, it is noteworthy that Altium Designer Mixed Simulation boasts the highest number of green circles and the lowest number of red circles and is on par with PSpice in terms of yellow circles. This suggests that Mixed Simulation is the optimal choice for simulation software. Additionally, i-charging is currently equipped with an Altium Designer license for schematic and PCB designs, as well as for the simulation interface. Therefore, Mixed Simulation only exhibits 2 red and 1 yellow balls, affirming its appropriateness as the premier simulation software for the company.

It is important to mention, however, that during the simulation phase, the "Manufacturers Encrypted Model" table parameter, designated by a red ball in the Mixed

Simulation column, proved to be vital in continuing with the simulation. As a result, an alternative simulation interface had to be selected. Although PSpice was deemed the second-best option in theory, obtaining another simulation interface license was not feasible. Consequently, LTspice, which offers nearly the same level of comprehensiveness as PSpice and is free of charge, was chosen as the next best alternative.

Chapter 3

Implementation Aspects

This chapter unveils the design of the SECC prototype circuit which detailed schematics are elaborated in Appendix D. Each schematic is accompanied by its specific objectives, detailed explanations, and justifications.

3.1 HW Architecture

The hardware architecture depicted in the block diagram illustrated in Figure 3.1, is thoroughly elucidated to guide and familiarize readers with the essential components, SoCs, communication interfaces, and other vital elements.

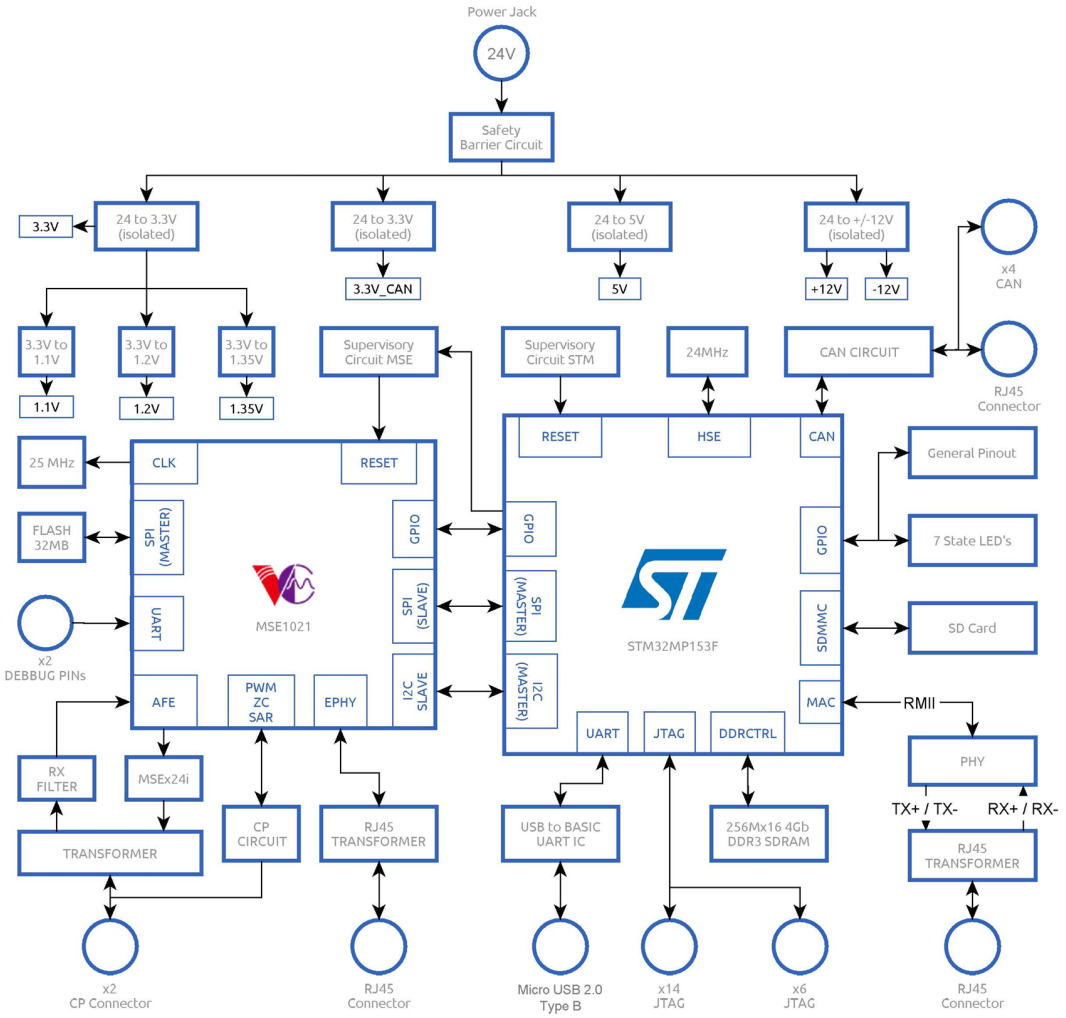


Figure 3.1: Block diagram of the Hardware Architecture

Throughout this chapter, the hardware architecture diagram is dissected into segments to introduce the corresponding designed schematics of each segment.

In the following sections, readers will have the opportunity to observe the inclusion of the following key elements in the schematics:

- **Test Points**: these are strategically integrated within the schematics for validation and circuit monitoring. They are positioned at critical circuit nodes where voltage measurement is paramount, such as voltage supplies or digital signals;
- **Status LEDs**: these LEDs are implemented to provide visual monitoring of specific node behavior, signal transmission or reception, and general debugging purposes;
- **Low Tolerance Resistors**: the majority of resistors utilized in this circuit exhibit a 1 % tolerance level. This adherence to tight tolerances represents a hallmark of good practices in schematic design.

3.2 Power Circuit

In this section, the Power circuit schematic of the SECC is outlined (Figure 3.2). Each green block refers to a single specific schematic sheet, presented in Appendix D.

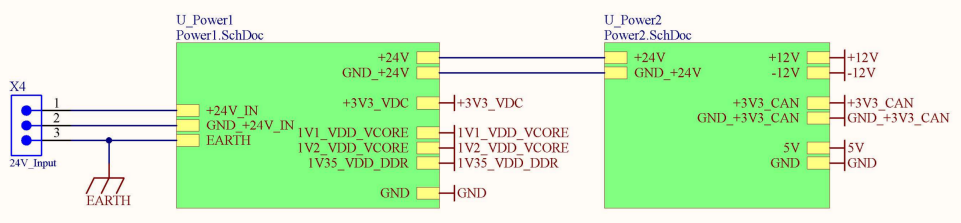


Figure 3.2: Power Block schematic circuit

Two critical considerations must be carefully addressed in the design and selection of components for this circuit:

- Determining SECC's SoC **voltage** supplies utilized throughout the entire circuit, as well as the voltage levels required for specific signals;
- Determining the circuit maximum consumed **current** for each voltage level, ensuring that the chosen DC/DC regulators fulfill the calculated maximum input and output values required for each DC/DC converter.

3.2.1 Voltage Levels and Current Supply

The circuit requires the following voltage supplies:

- **+/-12 V**: these voltage level supplies are imperative for powering the operational amplifier responsible for generating the square wave required by the IEC 61851-1 standard;
- **5 V**: this voltage level supply powers the HPGP line driver;
- **3.3 V**: this voltage level is the most commonly used in the circuit, as nearly every SoC operates at this voltage;
- **1.1 V**: this voltage level supply powers the PLC chip core;
- **1.2 V**: this voltage level supply powers the MCU core;
- **1.35 V**: this voltage level supply powers the Synchronous Dynamic Random-Access Memory (SDRAM).

To select the most suitable DC/DC converters for supplying the previously listed voltage values, it is imperative to carefully consider the maximum values of current

inputs and outputs. This ensures adherence to the specified maximum input and output values for each converter. Figure 3.3 illustrates the power segment of the Hardware architecture diagram with the maximum input currents of every SoC within the system.

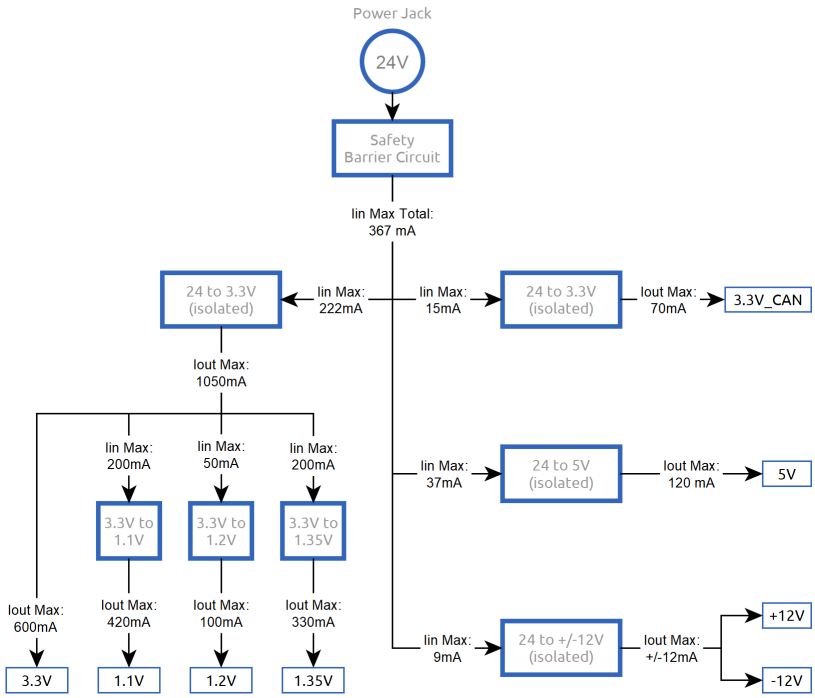


Figure 3.3: Maximum Input and Output currents

The current consumption values for each voltage level are the result of summing every maximum supply current value obtained from components datasheets, taking also into account the consumed power of components such as LEDs for each voltage supply output.

These consumption values were then utilized to calculate the maximum input current required by each converter using the following equations:

$$Vout * Iout = Pout$$

$$Pout/Efficiency = Pin$$

$$Pin/Vin = Iin$$

$$Iin * tollerance = Iin_{max}$$

These formulas utilize the output voltage and output current (calculated as explained in the preceding paragraph) of the DC/DC converter to derive the maximum output power value of the converter in question. This output power value is then divided by the minimum efficiency value provided in the datasheet of the converter for the desired voltages, yielding the maximum input power. Finally, this value is

employed to calculate the maximum current input value that the converter must support. By applying these formulas for every converter, the values depicted in Figure 3.3 are obtained.

3.2.2 DC/DC Converters

In accordance with project specifications mandating a 24 V circuit supply input, and after meticulous consideration of the calculated values for the required voltage levels, as well as the essential current inputs and outputs delineated in the preceding subsection, a thorough review has led to the selection of the DC/DC converters presented in the upcoming list.

It's imperative to underscore that each chosen DC/DC converter directly supplied by the external 24 V source is an isolated converter. This strategic choice has been made to fortify the circuit against any potential external faults.

- **PQQ6W-Q24-S3-S**: this 24 V to 3.3 V fixed regulated output boasts an input voltage range of 9 to 36 V, a maximum output current of 1350 mA, and a maximum input current value of 283 mA. Notably, the maximum current values depicted in Figure 3.3 align within the specifications provided in the PQQ6W-Q24-S3-S datasheet [45]. Represented in the figure below, this DC/DC converter is part of the PQQ6W series of regulated output converters typically supplied with a 24 V input voltage.

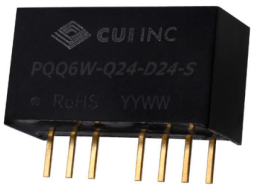


Figure 3.4: PQQ6W series DC/DC Converter [45]

- **PQQ6W-Q24-S5-S**: also a part of the PQQ6W series, this 24 V to 5 V converter offers an input voltage flexibility ranging from 9 to 36 V. It delivers a robust maximum output current of 1200 mA while consuming a maximum input current of 312 mA. It's worth nothing that the values illustrated in Figure 3.3 are within the specifications outlined in the DC/DC converter datasheet [45].

- **TPS746135PQWDRBRQ1**: this fixed output converter steps down 3.3 V to 1.35 V, boasting an input voltage range spanning from 1.5 V to 6.0 V. It is equipped with a maximum output current of 1 A and a peak output current value of 1.83 A. Notably, the values depicted in Figure 3.3 meticulously

align with the specifications outlined in the DC/DC converter datasheet [46]. Illustrated in the figure below, this converter is also a part of the TPS746-Q1 series, which encompasses two additional converters selected for this project and presented subsequently.

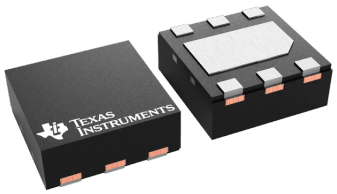


Figure 3.5: TPS746-Q1 series DC/DC Converter [46]

- **TPS74612PQWDRBRQ1**: belonging to the TPS746-Q1 series, this fixed output converter steps down 3.3 V to 1.2 V, covering an input voltage range from 1.5 V to 6.0 V. It is engineered with a maximum output current capacity of 1 A and a peak output current value of 1.83 A. It's worth nothing that the values illustrated in Figure 3.3 are within the specifications outlined in the DC/DC converter datasheet [46].
- **TPS74612PQWDRBRQ1**: part of the TPS746-Q1 series, this fixed output converter steps down 3.3 V to 1.1 V, encompassing an input voltage range from 1.5 V to 6.0 V. It is designed with a maximum output current capacity of 1 A and a peak output current value of 1.83 A. It is noteworthy that the values depicted in Figure 3.3 fall within the specifications detailed in the DC/DC converter datasheet [46].
- **A2412S-2WR2**: this 24 V to +/-12 V fixed regulated output boasts an input voltage range of 21.6 to 26.4 V, a maximum output current of +/-83 mA, and a maximum input current value of 104 mA [47]. Notably, the maximum current values depicted in Figure 3.3 align within the specifications provided in the A2412S-2WR2 datasheet [47]. Represented in the figure below, this DC/DC converter is part of the A_S-2WR2 series of fixed dual output.

Figure 3.6: A_S-2WR2 series dual output DC/DC Converter [47]

3.2.3 Power Schematics

This section presents a detailed description of the power block's implementation by introducing the Power Circuit segment. The segment under consideration showcases the 24 V input circuit alongside two DC/DC converters, as depicted in Figure 3.7.

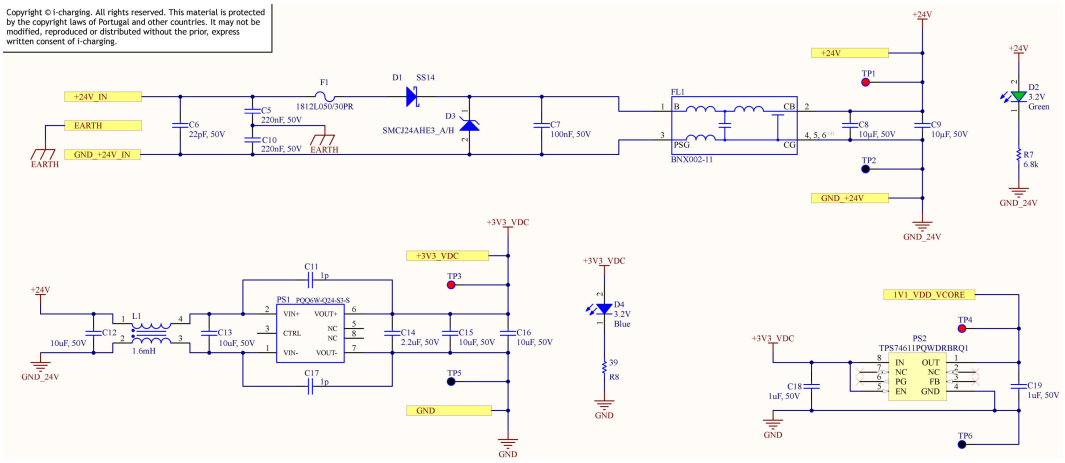


Figure 3.7: First segment of the Power circuit

In addition to highlighting protective measures against electrical faults, this segment features circuit filters designed to mitigate voltage and current fluctuations and noise. The key considerations and components of the segment are as follows:

- **TVS Diodes:** protect the circuit against voltage spikes by quickly diverting excess voltage away from sensitive components, safeguarding them from damage;
- **Schottky Diodes:** efficiently allow current flow in one direction with lower voltage drop compared to standard diodes, ideal for applications requiring high switching speeds;
- **Electromagnetic Interference (EMI) Filters:** reduce electromagnetic interference by attenuating unwanted high-frequency signals, ensuring compliance with regulatory standards and improving system reliability;
- **Capacitors:** store and release electrical energy, smoothing voltage fluctuations, filtering noise, and providing stability to power supplies and circuits.
- **PTC Resettable Fuse:** it is an electronic component that protects circuits from overcurrent conditions. Made of a thermally sensitive polymer, its resistance increases dramatically when exposed to excessive current, effectively limiting flow and preventing damage. Once the fault is resolved, it resets automatically, eliminating the need for manual intervention. Used widely in

electronics, it ensures system reliability by safeguarding against short circuits and overloads.

In Appendix D, other converters, similar to those depicted in 3.7, are arranged following the typical application suggestions in their respective datasheets, with capacitors and Common Mode Choke (CMK)s included. The Light-Emitting Diode (LED)s and Test Point (TP)s incorporation is justified as per the reasons outlined at the beginning of this chapter.

3.3 PLC chip, Peripherals and Comms

This section introduces the schematics for the MSE1021 HPGP chip, along with all necessary peripherals for establishing communication with the EV side. The hardware architecture depicted in this section comprises various blocks, as shown in Figure 3.8.

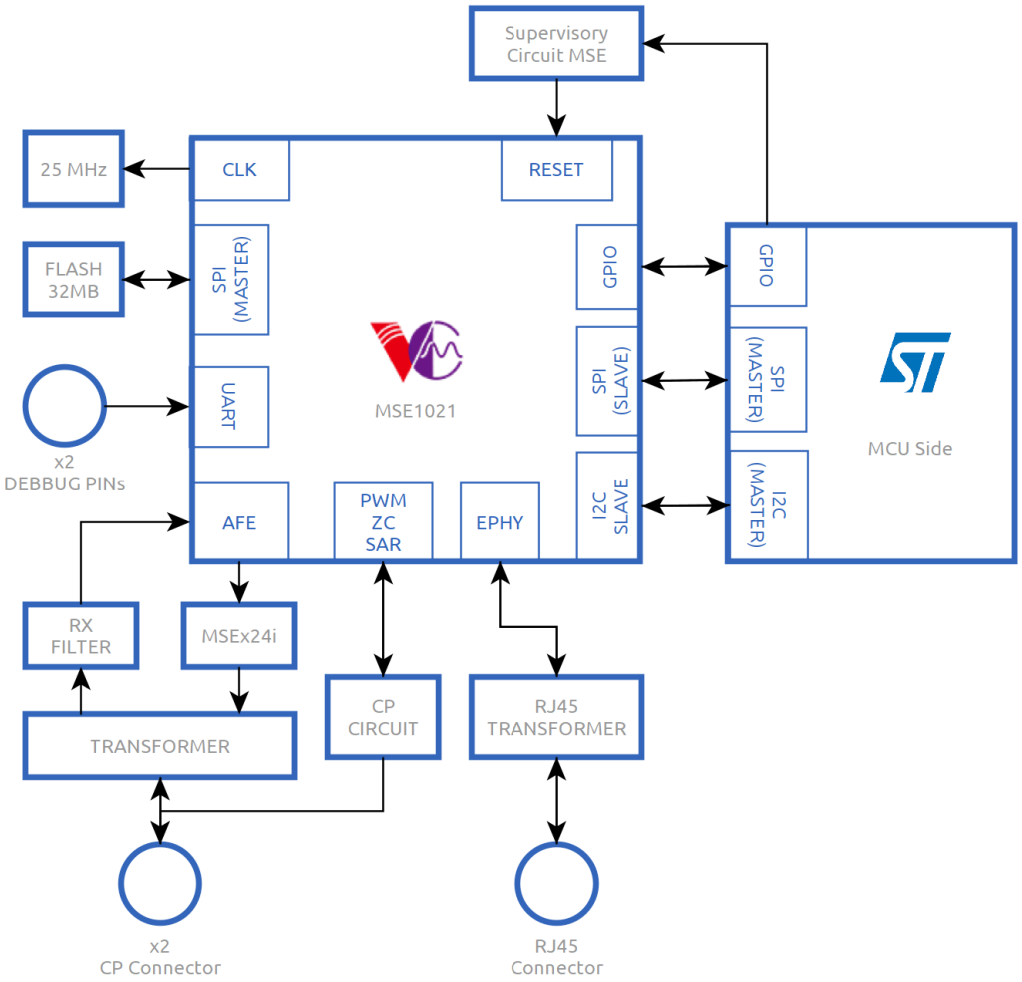


Figure 3.8: Hardware architecture - PLC chip blocks segment

3.3.1 CP Circuit - Digital Signal

The architecture presented in Figure 3.8 includes the CP Circuit block, which corresponds to the 5th sheet of the appendix D. This schematic illustrates the circuitry responsible for generating the PWM signal, as per the specifications outlined in Appendix A. This schematic represents the EV Supply Equipment side of the typical control pilot circuit presented on the IEC 61851-1 [7] (Figure 3.9).

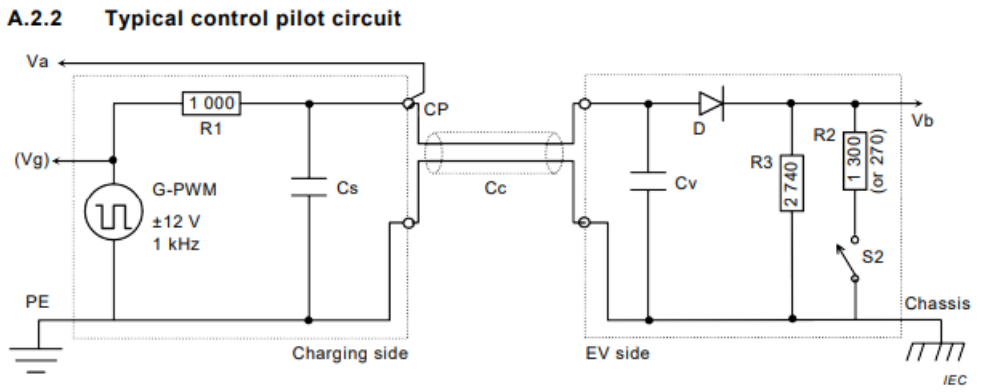


Figure 3.9: Typical Control Pilot Circuit presented on IEC 61851-1 - Anex A [7]

The primary objective of the circuit is to generate a diverse set of low-level signal states, as outlined in Table A.4 of the IEC 61851-1, by strictly adhering to the specifications laid out in the standard. A summary of the IEC 61851-1 table, which describes the charging states in question, is presented in Table 3.1. The circuit design has been developed with the express purpose of conforming to the project specifications by meeting part of the specified Appendix A requirements. The circuit implementation will ensure that it is capable of generating the required signal states in compliance with the IEC 61851-1 and SAEJ1772 standards.

Table 3.1: Charging states requests using PWM

State	Pilot High	Pilot Low	Frequency	Resistance	Charging State
State A	+12V	-	DC	-	Not Connected
State B	+9V	-12V	1kHz	2740Ω	EV Connected
State C	+6V	-12V	1kHz	882Ω	EV Charge
State D	+3V	-12V	1kHz	246Ω	EV Charge (Ventilation Required)
State E	0V	0	-	-	Error
State F	-	-12V	-	-	Unkown/Error

It is important to note that each state voltage level has a tolerance of +/- 1 V, and voltage levels between states are monitored to ensure that the digital signal is never unknown. Additionally, each state presented in table 3.1 consists of two

states: X1 and X2. The first state denotes that the PWM oscillator is off, while the second state denotes that the PWM is on.

After conducting a thorough analysis of the datasheets and application notes for MSE1021, as well as considering the project specifications, the final schematic design was determined based on several critical factors. In this regard, the circuit explanations are provided below, taking into account the aforementioned considerations.

For the purpose of this analysis, the Control Pilot circuit has been segmented into four distinct parts. In order to proceed with the analysis, it is essential to take into account the precise positions of the nodes Vg and Va, as illustrated in Figure 3.9. These nodes are of critical importance for their respective analyses and must be carefully considered.

PWM Generator

To generate the PWM signal, it is crucial to ensure that the signal high voltage level is +12 V while the low voltage level is -12 V. To achieve this, a Non-Inverting Comparator circuit was utilized (Figure 3.10).

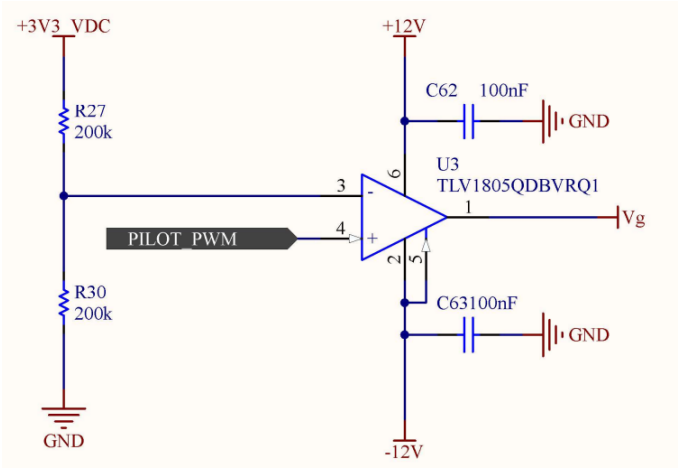


Figure 3.10: Control pilot schematic segment - PWM Generator

This circuit is relatively simple, featuring a configuration whereby VREF is linked to the inverting input. VREF represents the output voltage of a voltage divider comprising two equal high-resistance resistors. This arrangement configures VREF to be half of the 3.3 V voltage supply, which is equivalent to the high logical level of the designated plate number. As a result, whenever the plate number's PWM signal voltage exceeds the VREF value, the circuit outputs 12 V at point Vg. On the contrary, when the voltage level drops below the VREF value, the voltage at point Vg becomes -12 V. The selection criteria for the comparator were two-fold: ensuring rapid output rise and fall times, as stipulated by project specifications, with

a maximum allowable rise and fall time of 2 us at Vg, and ensuring that the supply voltage can accommodate the high and low thresholds of +/- 12 V. It is pertinent to note that this explanation does not account for the comparator tolerances.

Typical Control Pilot Circuit - EVSE Side

The control pilot schematic segment presented in Figure 3.11 presents the typical application circuit introduced in Figure 3.9.

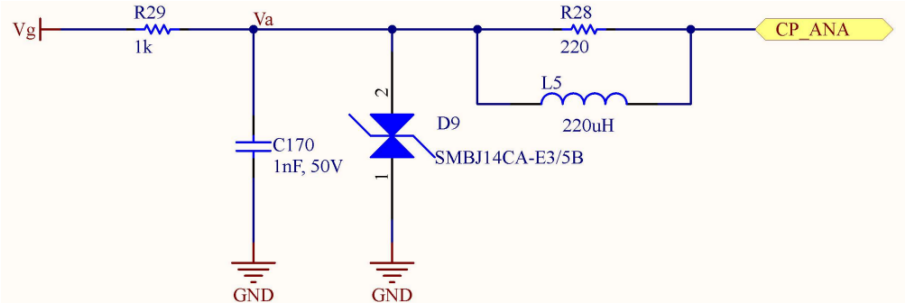


Figure 3.11: Control pilot schematic segment - Typical Application Circuit

Besides the typical application components, three others are added:

- **TVS Diode:** this diode aims to protect the circuit against voltage spikes;
- **Parallel of Resistor and Inductor:** this small circuit, consisting of a resistor and an inductor in parallel, serves as a safeguard for the control pilot circuit against current spikes caused by the noise emanating from the PLC. It is crucial to note that the resistor does not alter the voltage level of the line, as it would affect the voltage level of the states. This is because, once the inductor is fully magnetized, it behaves like a short circuit. The resistor is intended to dissipate the excess power generated by the spike when the inductor demagnetizes.

Control Pilot Duty Cycle Feedback

The acquisition of feedback regarding the duty cycle of the Control Pilot PWM is necessary for the proper functioning of the MSE1021. To this end, attention must be paid to the segment of the control pilot schematic that is responsible for converting the control pilot PWM signal into a PWM signal with logic levels that an analog input of the MSE1021 can read. Figure 3.12 illustrates this segment of the schematic in detail.

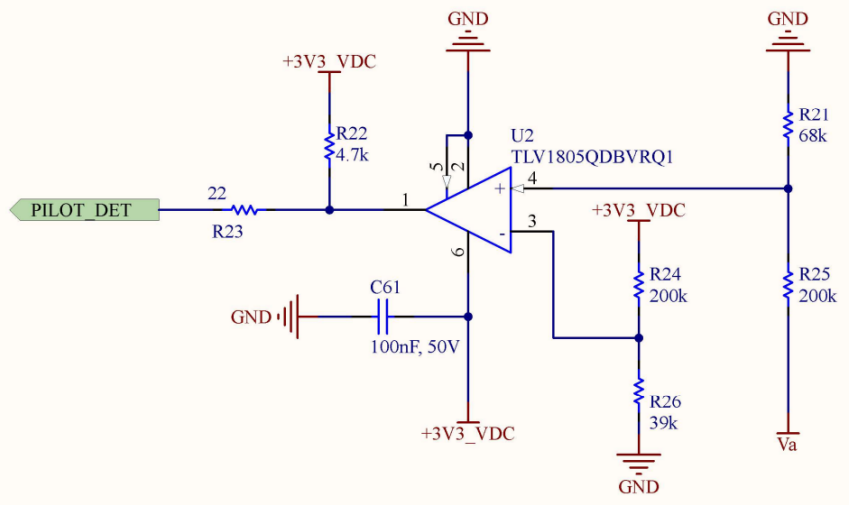


Figure 3.12: Control pilot schematic segment - Duty Cycle Feedback

This circuit functions as a comparator circuit, wherein the objective is to output a high logic level when the voltage on node Va is positive and a low logic level when the voltage on the same node is negative. It is noteworthy that the VREF in this scenario is not directly connected to the ground but is instead connected to the output voltage divider between R24 and R26, resulting in a VREF value of approximately 0.5 V. This is because a tolerance must be incorporated to debounce and mitigate the effects of logic-level changes. On the other hand, the voltage divider output between R21 and R25 aims to consistently produce a value lower than 3.3 V even when the Va node voltage is at its maximum. This is because the maximum value accepted as input on the Non-inverting input of the comparator is 3.3 V, disregarding tolerances. If the divisor output level exceeded that maximum input value, the high threshold of the control pilot digital signal would not be detected. It is worth taking note of the fact that a 22 Ω resistor is utilized in series between the output of the comparator and the input of MSE1021. This serves to isolate MSE1021 from the high-output impedance of the comparator, as well as to offer protection to the MSE during a fault condition.

Control Pilot Voltage Feedback

In addition to the control pilot duty cycle feedback, the MSE1021 system also necessitates the control pilot feedback voltage. Figure 3.13 illustrates the circuitry that transforms the control pilot voltage, which ideally lies within +/-12 V, into a voltage range spanning from 0 to 3.3 V. This voltage range serves as the input for the MSE1021 ADC.

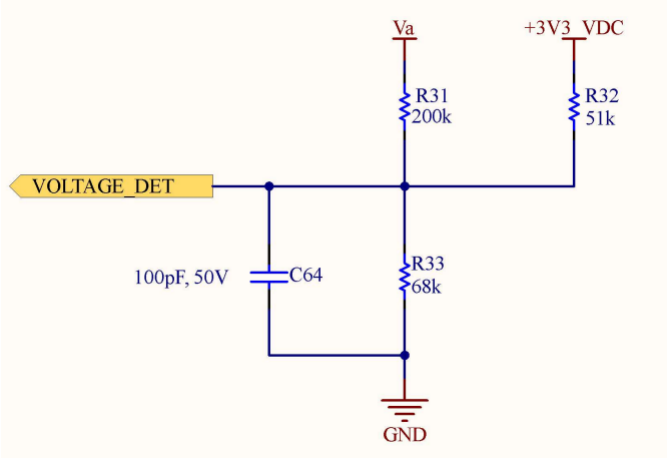


Figure 3.13: Control pilot schematic segment - Voltage Feedback

In order to maintain a low current value, high resistance values were assigned to the resistors. Consequently, R1 was established as a 200 kΩ resistor. To determine the values of the other two resistors, voltage dividers were calculated for two scenarios.

- **VOLTAGE_DET = 0 V:** in this scenario, the differential voltage across R33 is 0 V. As a result, the calculation of the resistance value for R32 was conducted using the following equations:

$$VR_{32} = (Va - 3V3) * \frac{R_{32}}{R_{32} + R_{31}} \iff$$
$$-3.3 = -16.3 * \frac{R_{32}}{R_{32} + 200\,k} \iff$$
$$R_{32} = 50.7\,k\Omega \approx 51\,k\Omega$$

  It is imperative to note that to maintain tolerance on the ADC input reading, Va was established as -13 V. This is to ensure that the VOLTAGE_DET does not drop below 0 V.

- **VOLTAGE_DET = 3.3 V:** in this scenario, the differential voltage across R32 is 0 V. As a result, the calculation of the resistance value for R33 was conducted using the following equations:

$$VR_{33} = (Va) * \frac{R_{33}}{R_{33} + R_{31}} \iff$$
$$3.3 = 12 * \frac{R_{33}}{R_{33} + 200\,k} \iff$$
$$R_{33} = 68\,k\Omega$$

It is crucial to note that in order to maintain tolerance on the ADC input reading, Va was established at 13 V. This was done to ensure that the VOLTAGE_DET does not exceed 3.3 V.

The application of Kirchhoff's laws enables the conversion of any voltage value, Va, to a voltage value that the MSE1021 can read. For instance, to determine the corresponding VOLTAGE_DET value when the charging state is in state B, and the control pilot high voltage is 9 V, the following calculations must be conducted:

1^{st} law

$$I_{R3} = I_{R1} + I_{R2}$$

2^{nd} law

$$\begin{cases} V_a & - & R_{31} * I_1 & - & R_{33} * (I_1 + I_2) & = & 0 \\ 3V3 & - & R_{32} * I_2 & - & R_{33} * (I_2 + I_1) & = & 0 \end{cases}$$

where I_1 is the loop 1 current and I_2 is the loop 2 current. The values of the currents in the respective loops can be obtained by substituting the variables with their respective values, as follows:

$$\begin{cases} 9 & - & 200 * I_1 & - & 68 * (I_1 + I_2) & = & 0 \\ 3.3 & - & 52 * I_2 & - & 68 * (I_2 + I_1) & = & 0 \end{cases} \iff$$

$$\begin{cases} I_1 & = & 31\,\mu A \\ I_2 & = & 9.89\,\mu A \end{cases}$$

Finally, is possible to calculate the VOLTAGE_DET value when $V_a = 9\,V$:

$$VOLTAGE\_DET = R_{33} * (I_2 + I_1) \approx$$

$$VOLTAGE\_DET = 68 * (0.031 + 0.00989) \approx$$

$$VOLTAGE\_DET = 2.77\,V$$

In summary, the aforementioned calculation elucidates the methodology employed for voltage conversion and provides the reader with a comprehensive understanding of the circuit's functionality. The calculation's explication allows for a thorough comprehension of the intricate workings of the circuit.

3.3.2 Control Pilot - PLC

The sixth sheet of Appendix D presents the PLC transformer circuit, which is responsible for receiving the PLC signal from the EV side and transmitting the signal generated by the MSE1021. Given the complexity and sensitivity of this circuit, the

schematic circuit was adapted from information obtained from application notes, datasheets, and reference schematics provided by VertexCom [30]. The circuit includes:

- **MSEX24-i [30]:** MSEX24-i is a dedicated single port differential line driver that has been specifically designed for applications in PLC and HomePlug GreenPHY. The device is capable of handling heavy line loads while maintaining high levels of linearity that are essential in PLC links;
- **BMU6201NL [48]:** BMU6201NL serves as a vital component in powerline communication systems, allowing data transmission over existing power lines. Specifically designed for HomePlug Green PHY applications, it ensures efficient and reliable communication within smart grid systems, home automation, industrial control, and smart metering. This transformer facilitates seamless integration, maintaining signal integrity while meeting the industry and communication standards for interoperability and compatibility;
- **Filters and protection circuits:** this circuit employs an array of capacitors, inductors, resistors, and TVS diodes, strategically positioned to fulfill multiple critical functions. These components serve the purpose of filtering, both for EMI and Electromagnetic Compatibility (EMC), ensuring the integrity of signals by mitigating noise and interference. Additionally, they play a pivotal role in safeguarding against electrical faults, with capacitors and TVS diodes protecting against voltage spikes and transient surges. Furthermore, inductors, capacitors, and resistors contribute to frequency filtering, allowing selective passage of desired frequencies while attenuating others, thus optimizing signal quality and system performance. This comprehensive approach to component integration not only enhances the reliability and efficiency of the circuit but also ensures its compliance with stringent industry standards for electromagnetic compatibility and electrical safety.

3.3.3 Peripherals and Comms

This section provides a comprehensive overview of the peripherals and communication interfaces that are utilized by and required for the MSE1021. The information presented is intended to offer a detailed understanding of the communication mechanisms and supporting hardware components that facilitate the optimal functioning of the MSE1021.

Peripherals

- **Crystal:** 25 MHz Crystal. The external capacitors values connected to the crystal are calculated using the following formula:

$$C = 2 * (CL - Cstray)$$

Here, CL denotes the capacitance load of the oscillator, and Cstray refers to the unavoidable capacitance between nearby conductors. Therefore, substituting the variables for the respective values, the capacitance of the external capacitors is given by:

$$C = 2 * (18 - 5) = 26\,pF$$

The closest common value of capacitance to 26 pF is 27 pF, which is the defined value;

- **NOR Flash Memory:** A 32-megabit NOR Flash spiFlash is used for boot purposes;
- **Supervisory Circuit:** a 5-pin SoC supervisory circuit that combines reset output, watchdog, and manual reset input functions. The supervisory circuit of the PLC chip, as detailed in Appendix D, includes a watchdog timer that requires periodic resetting by the MCU. Failure to do so will result in the triggering of the watchdog timer and subsequent reset of the MSE;
- **Dip Switch:** a 9-Position Dip Switch for bootstrapping. The dip switch allows for the configuration of MSE1021. For instance, by adjusting a specific switch on the dip switch, users can choose between different communication interfaces with the MCU, such as SPI or Ethernet.

Communication Interfaces

- **SPI:** 1x SPI communication interface between the MCU and the MSE1021;
- **UART:** 1x UART for debugging purpose using 2 pins header;
- **I2C:** 1x I2C communication interface used for bootloader download under the circumstance where the communication interface between the MCU and the MSE1021 is SPI, and the MSE1021 SoC requires booting from the host (MCU);
- **Ethernet:** 1x 10/100 integrated Ethernet PHY interface which facilitates a PHY-to-PHY connection. This interface is directly linked to an RJ45 female

Ethernet Connector, equipped with an integrated transformer to ensure complete isolation.

3.4 MCU, Peripherals and Comms

This section approaches the schematics of the Microcontroller Unit (MCU), along with all necessary peripherals for establishing communication with the charger side. The hardware architecture depicted in this section comprises various blocks, as shown in Figure 3.14.

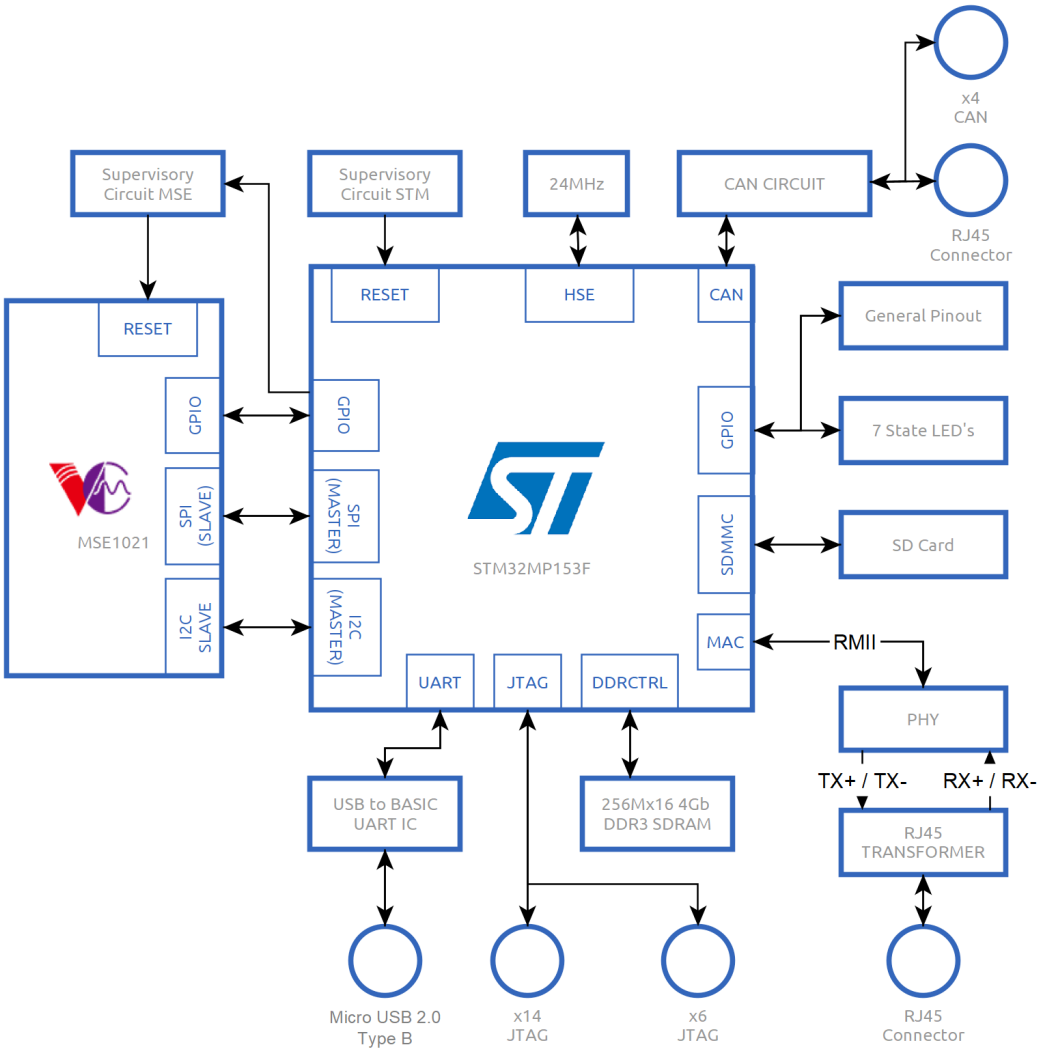


Figure 3.14: Hardware architecture - MCU blocks segment

3.4.1 Peripherals

This sub-section provides an overview of the MCU peripherals, which are essential for various applications, including establishing communication interfaces and resetting

the MCU, for instance.

Supervisory Circuit

A 5-pin SoC supervisory circuit that combines reset output, watchdog, and manual reset input functions. The SECC circuit employs two MAX823SEUK+T [49]. This supervisory circuit, depicted in Figure 3.15, is in charge of resetting the MCU. Notably, the MCU undergoes a reset only when S5 is open (not connected to the ground) and momentary button S4 is pressed. When S5 is closed, the supervisory circuit remains inactive and does not impact the MCU. Consequently, in this setup, the external watchdog feature is not utilized by the MCU.

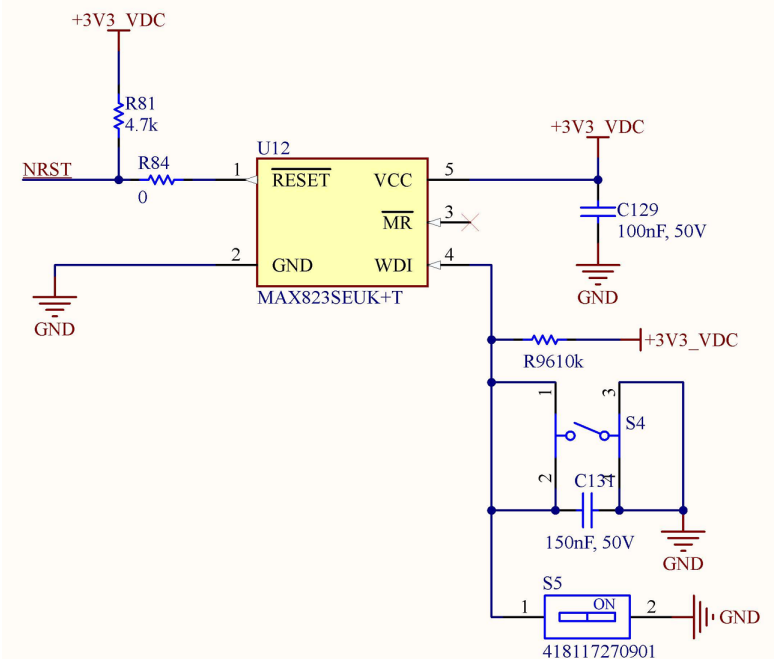


Figure 3.15: Supervisory Circuit present on SECC's schematic

Crystal

A 24 MHz external crystal. The values of the external capacitors connected to the crystal are determined using the formula provided earlier in this document, in Sub-subsection 3.3.3.

CAN Circuit

The CAN circuit, presented in Appendix D, can be segmented into three distinct parts to facilitate comprehensive explanation:

- **Isolation Circuit:** two FODM8071R2 [50] optocouplers were implemented for crucial electrical isolation between the SECC circuit and the external CAN

bus, as is possible to observe in Figure 3.16. This isolation prevents noise, ground loops, and potential high-voltage spikes from damaging sensitive components, thus enhancing the system's robustness and safety. Beside, signal integrity is maintained by isolating the CAN bus signals from the rest of the circuit, ensuring that any interference or noise on the bus does not affect the microcontroller and vice versa. By incorporating these optocouplers, both the Transmit (TX) and Receive (RX) lines are effectively protected, ensuring comprehensive isolation and protection for the CAN interface circuit.

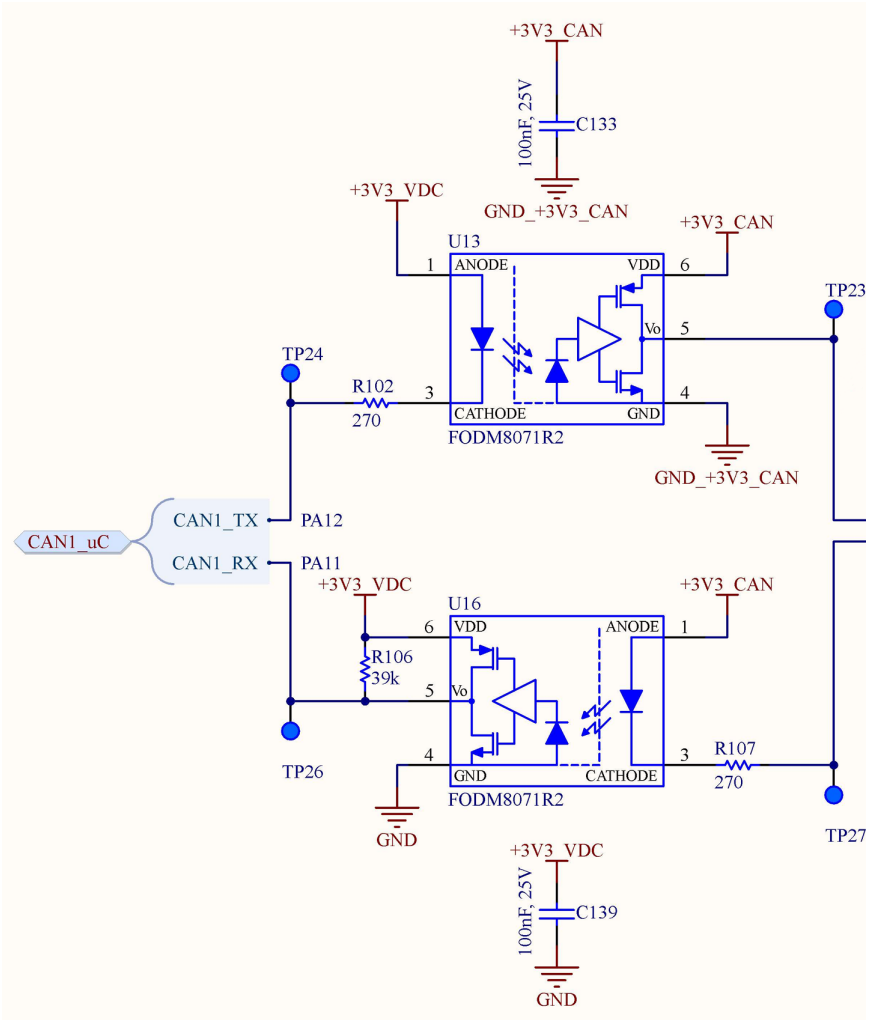


Figure 3.16: Isolation circuit for CAN interface

- **CAN Transceiver:** in Figure 3.17 it's possible to observe that one LTC2875 [51] CAN transceiver is employed within the circuit to facilitate communication between the MCU and the physical CAN bus. This component efficiently converts digital signals originating from the MCU into differential CAN bus signals, and conversely, thereby enabling the transmission and reception of data. Its essential functionalities encompass signal conversion, error detection,

and bus arbitration, all of which collectively serve to ensure the reliability and efficiency of communication within the system.

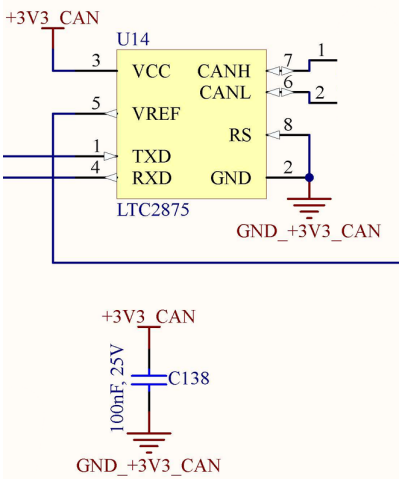


Figure 3.17: CAN bus transceiver in CAN circuit

- **Filter Circuit**: the figure labeled as 3.18 depicts the CAN interface filter circuit designed to mitigate electromagnetic interference (EMI) and ensure signal integrity. The purpose of this circuit is to suppress noise and unwanted signals that can disrupt communication on the bus, and reliable data transmission of data between nodes is ensured. More details about this circuit are presented in Subsection 4.2.2.

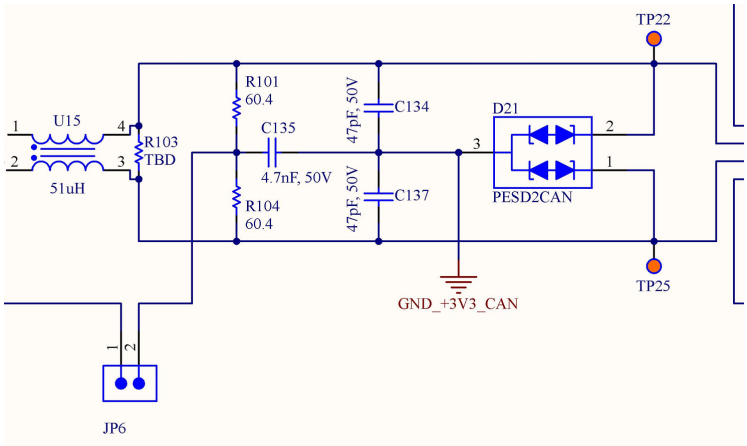


Figure 3.18: CAN bus transceiver in CAN circuit

General Purpose I/O Pinout

This block outlines the allocation of pins designated for potential expansion and various general-purpose input/output operations. These pins can be repurposed as needed to accommodate evolving project requirements.

Status LEDs

Utilized for signaling different system states or activities, status LEDs can be programmed to indicate normal circuit behavior, data transmission, or serve as general-purpose indicators, providing users with valuable visual feedback on system operation.

SD Card Interface

The SD card interface, detailed in Appendix D, plays a crucial role in this circuit design for embedded Linux. It provides essential storage for the operating system, configuration files, and user data. The interface's boot capability from the SD card facilitates data storage and retrieval, significantly improving the flexibility and expandability of embedded system designs.

Ethernet Interface

The Ethernet block in Figure 3.14 comprises an Ethernet transceiver, namely the DP83826IRHBR [52], which is a critical component in communication interface hardware. The transceiver, also known as a Physical Layer, facilitates the transmission and reception of data over Ethernet cables. It fulfills this function by converting digital data from the device into signals that can be transmitted over the network and vice versa.

The project leverages the Reduced Media Independent Interface (RMII) interface, a standard that enables communication between the Ethernet transceiver and the Ethernet Media Access Controller (MAC) layer of the MCU using fewer pins. This standard simplifies design and reduces costs while supporting high-speed data transfer and maintaining a compact and efficient connection, aligning with the application's requirements.

Furthermore, the transceiver controls the state LED situated on the RJ45 connector, which the transceiver interfaces with the exterior. These LED indicate the network connection's status, providing visual feedback on link activity and speed. This feature enhances the ease of monitoring and troubleshooting the network.

DDR3 SDRAM Memory

The memory block depicted in Figure 3.14 represents the IS43TR16256BL-107MBLI [53] (Figure 3.19), a high-capacity 4 GB DDR3 SDRAM module with a 256 MB x 16 configuration. This module can operate at speeds of up to 933 MHz (DDR3-1866) and boasts low column address strobe latency, ensuring rapid and efficient data processing. Notably, its design prioritizes energy efficiency, operating at 1.5 V, thus rendering it suitable for use within applications constrained by power requirements.

This particular memory module is esteemed for its reliability and stability facilitated by robust error-correction capabilities integrated into the circuit, offering essential storage and data handling capabilities. For a comprehensive understanding of its integration and functionality within the overarching system architecture, detailed schematics, pin mappings, and configuration settings are provided in Appendix D.

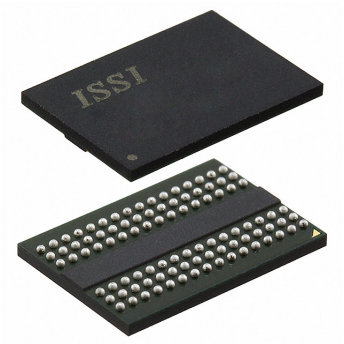


Figure 3.19: SDRAM - DDR3L Memory IC 4 GBit [53]

JTAG

The block diagram in Figure 3.14 displays two JTAG connectors, both of which are male box headers. One connector has 6 pins (Figure 3.20), while the other is equipped with 14. This difference is because some board debuggers and programmers come with a 6-pin connector, while others may have a 14-pin connector. Joint Test Action Group (JTAG) interfaces are essential for debugging, testing, and programming microcontrollers. They enable access to internal registers and memory and support step-by-step code analysis by developers.

Figure 3.20: 6 pin straight header [54]

UART to USB

In Figure 3.14, the UART to USB block represents the FT230XS [55] Integrated Circuit (IC) along with the surrounding circuitry detailed in Appendix D. The FT230XS (Figure 3.21) is a USB-to-UART interface IC manufactured by FTDI Chip. It provides a convenient bridge between Universal Asynchronous Receiver-Transmitter (UART) serial interfaces and Universal Serial Bus (USB) connections.

This transceiver facilitates communication between the MCU equipped with UART capabilities and a host computer or other USB-enabled devices. Detailed schematics, pin configurations, and implementation guidelines for the FT230XS and its associated circuitry can be found in Appendix D, providing insights into its integration and functionality within the overall system architecture.

Figure 3.21: FT230XS USB-UART converter [55]

3.4.2 Communication Interfaces

The elements constituting the SECC circuit have been previously delineated. In this section, the communication interfaces established by these aforementioned components are presented.

- **SPI:** A singular SPI communication interface is provided for interfacing with the MSE1021.
- **Ethernet:** The RMII 10/100 Ethernet stands as a protocol standard that simplifies communication between Ethernet transceivers and MAC (Media Access Control) layers in networking devices. Recognized for its diminished pin count, it renders itself space-efficient and cost-effective, making it a prevalent choice in routers, switches, and IoT devices.
- **CAN**: The Controller Area Network (CAN) serves as a robust and widely utilized communication protocol, primarily within automotive and industrial applications. It facilitates communication between microcontrollers and devices sans host computer dependency. Distinguished by its reliability, real-time capabilities, and fault tolerance, it finds suitability in critical systems such as vehicle control units and industrial automation.

  CAN leverages a differential signaling scheme to transmit data over two wires: CAN High (CANH) and CAN Low (CANL). This differential signaling ensures noise immunity and facilitates communication over extensive distances. CAN addresses a wide spectrum of application requirements by supporting diverse data rates ranging from 10 kbps to 1 Mbps.

  A notable characteristic of CAN is its prioritized message-based architecture. Messages on the bus are attributed identifiers, thus enabling devices to prioritize and filter incoming data based on their relevance. This ensures efficient

utilization of the bus bandwidth and precise control over communication traffic.

- **USB:** USB, a ubiquitous interface standard for connecting devices to computers and host systems, offers hot-swapping, plug-and-play functionality, and high data transfer rates. With a repertoire of data transfer modes and connector types, USB accommodates a wide array of peripherals, ranging from basic input devices to high-speed external storage solutions, thereby revolutionizing device connectivity in modern computing and consumer electronics.

Chapter 4

Debug, Evaluation and Test

This chapter elaborates on the steps that follow the circuit design phase, starting from validating the initial version of the schematic to simulating and verifying the final schematic. This stage includes crucial phases that are vital to the project success.

- **Validation:** in this phase, using the validation tool in Altium Designer, customizable error reports resolved numerous errors, including duplicate components and connection incompatibilities not detected during the schematic design phase.
- **Evaluation:** during this phase, the i-charging hardware team evaluated the final schematic and proposed changes to ensure proper circuit functionality.
- **Testing:** during this lengthy and complex phase, the relevant schematic blocks that were deemed valuable to analyze were simulated using the simulation software Mixed Simulation and LTSpice. Various types of simulations were conducted to verify the circuit behavior with temperature and voltage variations (due to tolerances), to identify rise and fall times of specific and crucial instants defined in the standard, among other simulations. In this final phase, the values and signals obtained in the simulations were compared and validated with the known values in the requirements and standards. If all time intervals, voltage values, and other conditions are met, the circuit is validated and finalized.

4.1 Debug and Evaluation

This section presents the debugging and evaluation phases conducted before running the circuit simulations.

Debug

Before moving on to PCB design, it is important to thoroughly review the schematic design for potential incompatibilities, duplicated components and other errors. To achieve this, a validation process should be conducted. Altium design rule-checking engine can be used to perform a comprehensive schematic debug, which will generate a list of all detected errors and warnings in the "Messages" panel. Each warning and error will be accompanied by a location link to the specific schematic sheet where it was detected [56]. Figure 4.1 showcases five instances of errors and warnings that were output in the messages panel of the Altium Designer project schematic. These errors were intentionally introduced by eliminating a single schematic net, as demonstrated in Figure 4.2, for the purpose of exemplification. It is important to note that all warnings and errors in the project schematic had been addressed at this point.

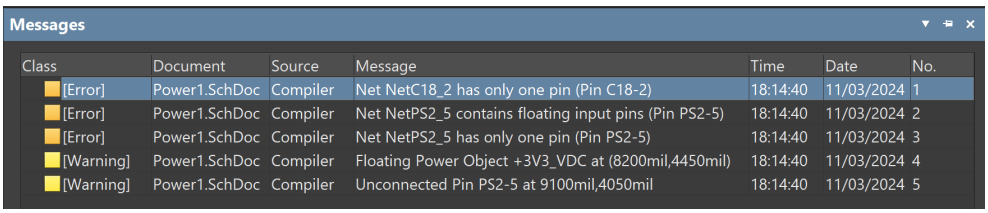


Figure 4.1: Altium Designer's Message panel

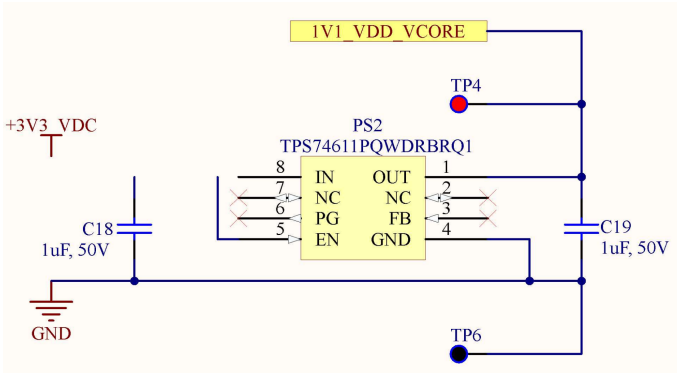


Figure 4.2: Intentional error on Power schematic

As mentioned earlier, errors and warnings are inherently tied to the location where they were detected. When double-clicking on the second error in the Message panel depicted in Figure 4.1, the corresponding schematic net where the error occurred is automatically zoomed in, as demonstrated in Figure 4.3.

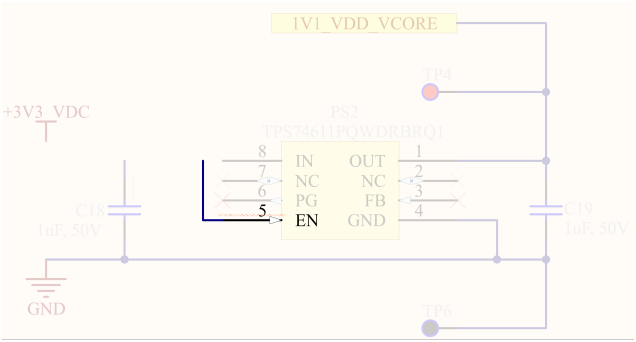


Figure 4.3: Intentional error highlighted on Power Schematic

Altium Designer's schematic rule checking process allows users to customize their error reports. This allows for fine-tuning each specific violation to be reported as a warning, error, fatal error, or not reported at all. The software is fully adjustable, providing users with the flexibility to meet their unique needs and requirements. It is noteworthy that the error reporting mechanism adopted for the project was the pre-defined one, established and refined by the Schematic and PCB design team. As previously mentioned, prior to proceeding to the subsequent phase of the project, every error and warning was meticulously reviewed and addressed.

Evaluation

In this project phase, a detailed and extensive analysis was carried out in conjunction with colleagues from the Schematic and PCB design teams. The objective was to uncover any limitations or incompatibilities that may have eluded Altium Designer's validation process. Among others, examples include:

- the possibility of component package sizes being too small for certain high-current points, necessitating the use of larger components for more effective heat dissipation;
- incorrect connections between communication interfaces of integrated circuits;
- lack of protection components for certain circuits;
- verification of signal conditioning circuits.

A significant proportion of the identified constraints were found to be associated with the dimensions of the components package.

After the evaluation phase was successfully completed, the subsequent stage of testing to simulate the project schematic was initiated.

4.2 Simulation Tests

The hardware diagram in Figure 4.4 is divided into blocks, each of which is covered by an outline-colored rectangle. Each color represents specific characteristics that were carefully considered before deciding whether or not to simulate the respective block circuit.

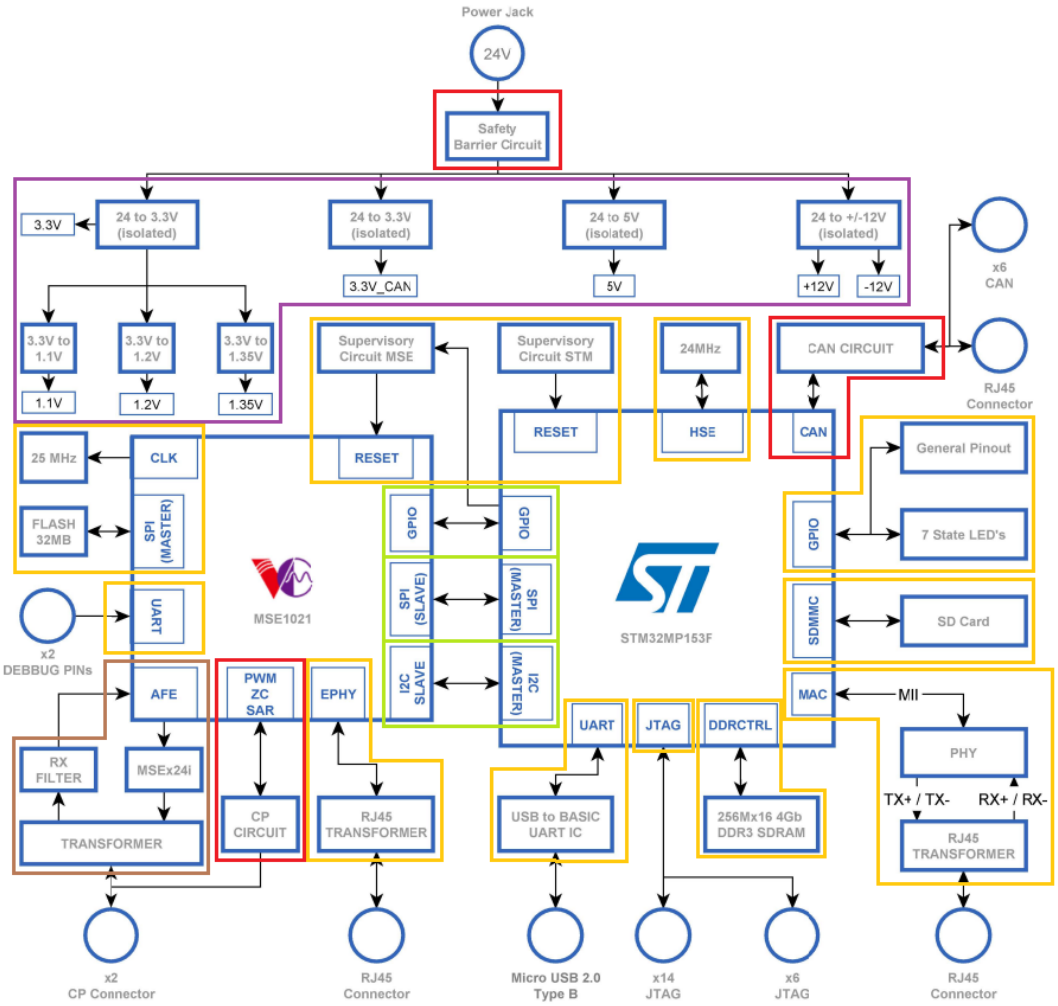


Figure 4.4: Red rectangles signaling which parts of the circuit were simulated

The colors in Figure 4.4 represent the following aspects:

- **Purple:** there are no available SPICE models online. When analyzing circuits that work with the output voltage of any of these DC/DC regulators, the tolerances are taken into consideration;
- **Green:** these point-to-point communication interfaces use almost no electronic components between the devices and involve signals purely generated

by the certified MCU and PLC chip. The interfaces and connections are established following the datasheets and application notes;

- **Yellow:** selects peripherals circuits that involve components lacking spice models or simple parts that include SPICE models, such as LEDs. These circuits are not simulated once the hardware interface complexity is small and do not need additional signal processing circuits. The interfaces are designed based on information from datasheets, application notes, and development boards;

- **Red:** the circuits are not typically found in datasheets or application notes. They are instead user-designed signal conditioning circuits. As a result, they consist of a larger number of electronic components chosen and assembled by the user and require simulation in order to test their behavior;

- **Brown:** this particular section of the diagram exhibits some of the characteristics mentioned earlier in the list. It contains components for which SPICE models are not available online, as well as subjective signal conditioning circuits that are highly intricate and contain numerous EMI and EMC filters. The circuit was adapted from an evaluation board schematic (confidential document provided by the official PLC chip manufacturer), and the complexity of the signals waveforms input and output by this circuit makes them nearly impossible to replicate. Due to the prevailing limitations, it was decided not to conduct any simulation analysis of this segment.

It is now possible to comprehend the selected segments of the circuit that were scrutinized, along with the underlying rationale for their simulation. The outcomes of the simulations for the enclosed portion of the circuit, demarcated by a red-colored rectangle, are elaborated in the subsequent subsections, providing a detailed analysis of the previous results.

4.2.1 Control Pilot Circuit

The subsequent subsection presents the simulation circuit for the control pilot. Figure 4.5 illustrates the circuit that aims to replicate the final SECC schematic Control Pilot (CP) circuit presented in chapter 3. However, the simulation circuit was modified to entirely replicate the typical control pilot circuit illustrated in IEC 61851-1 (Figure 4.6) in order to simulate the control pilot circuit for the SECC side of this project. Therefore, the circuit segment enclosed by the bottom red box represents the circuit of the right side in Figure 4.6, and it is meant solely for simulation purposes, as are the four voltage sources.

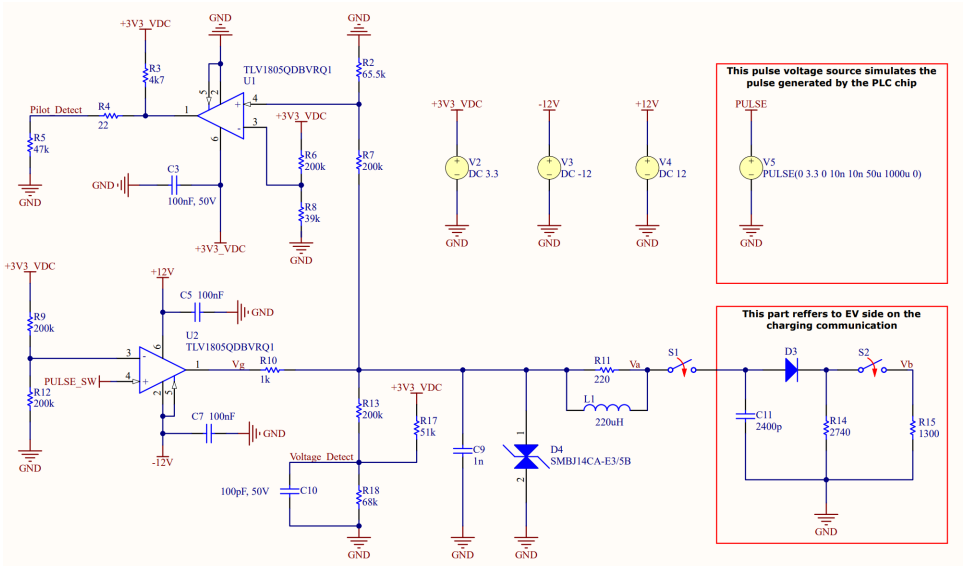


Figure 4.5: Control Pilot simulation circuit

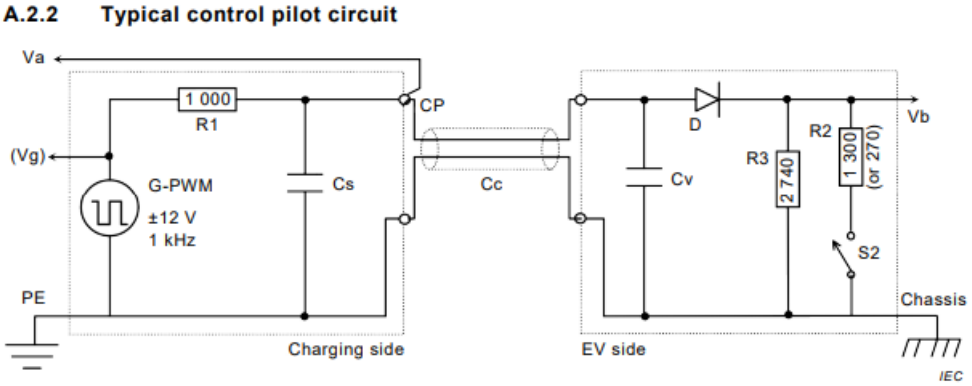


Figure 4.6: Typical Control Pilot Circuit presented on IEC 61851-1 - Anex A [7]

As indicated in Figure 4.5, the pulse (the PWM signal with a duty cycle of 5 %) is actually generated by the HomePlug Green Phy HPGP chip from VertexCom. However, it is not possible to simulate the signal as there is no simulation SPICE model available for the chip. Yet, it is known that the HPGP chip MSE2021 is compliant with IEC standard 61851-1. To create the signal, a voltage source with an amplitude of 3.3 V, a frequency of 1000 Hz, and a duty cycle of 5 % is used. The intention is to replicate the signal that the HPGP chip generates. The values used to create this signal are confirmed by official and confidential documents from VertexCom.

Before presenting the simulations, some initial considerations:

- every simulation that do not have an indication of the temperature at which they were simulated were carried out at 25 °C;

- the simulation SPICE models of the OP AMPs were taken from official websites and refer exactly to the model used in the circuit;
- the schematic capacitors presented also have their official simulation SPICE model associated to them. Those models are provided by Wurth, on the official manufacturer's website [57];
- All other components are from the Altium Designer Simulation generic components library.

Following these considerations, a few simulation results will be presented in accordance to the project specifications.

Voltage on point Vg

According to the project requirements presented in table 4.1, the static voltage at point VG of the PWM generator circuit, when the circuit is open (the vehicle is not plugged), should have typical values of -12 V and +12 V, with the respective tolerances provided in table 4.1.

Table 4.1: Specifications for open circuit voltage on point VG

ID	SPECIFICATION	STANDARD	CHAPTER/POINT	DEVIATION ACCEPTED	CHARGING SIDE
8	Generator open circuit positive voltage should have typical value of 12V	IEC 61851-1 / SAEJ1772	A.3 - Table A.2 / 5.2 - Table 4	11,4V to 12,6V	EVSE
9	Generator open circuit negative voltage have typical value of -12V	IEC 61851-1 / SAEJ1773	A.3 - Table A.2 / 5.2 - Table 5	-11,4V to -12,6V	EVSE

The transient analysis shown in Figure 4.8 was performed with the configurations presented in Figure 4.7. Enough signal cycles are plotted to show the stability and accuracy of the voltage on point Vg.

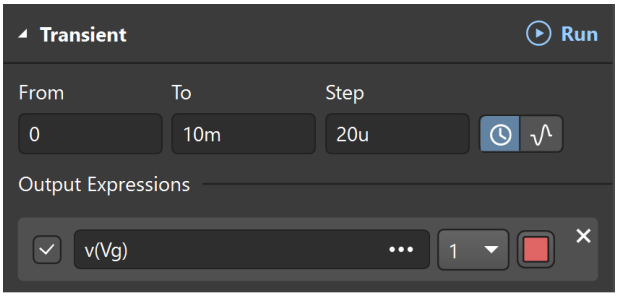


Figure 4.7: Transient analysis configuration

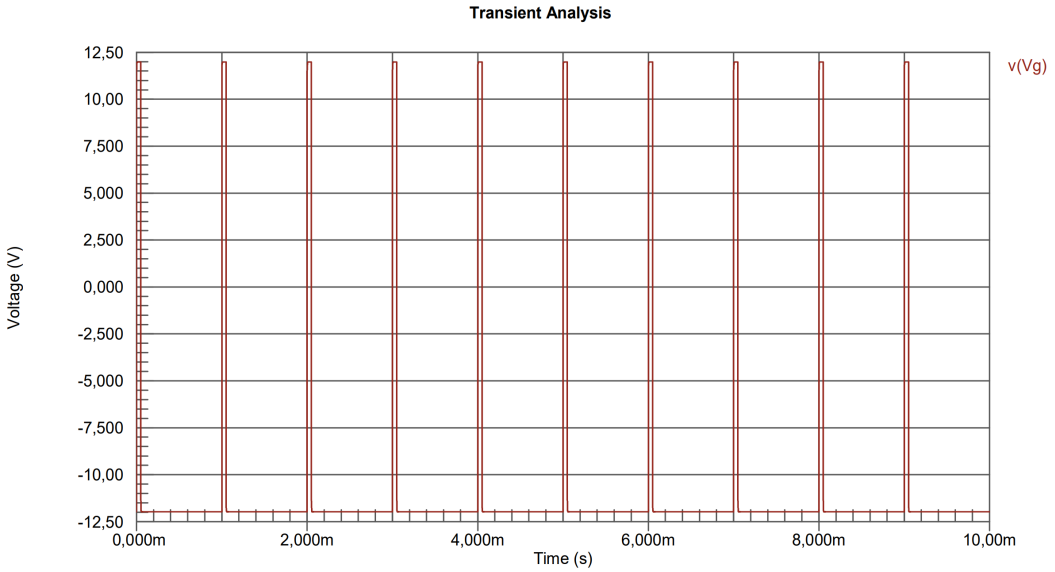


Figure 4.8: Transient simulation result on point Vg with base and top line measurements

The analysis of Figure 4.8 shows that the voltage on point Vg has a maximum value of 11.95 V and a minimum value of -11.97 V. These values fall well within the specified tolerance limits, indicating that requirements 8 and 9 have been met.

It is stated in the IEC standard 61851-1 and SAEJ1772 (the US equivalent of IEC61851-1 standard) that the PWM generator circuit must produce a pulse signal with rise/fall time of less than 2 μ sec (table 4.2). The measurement of rise time is the time it takes for the pulse's leading edge to rise from its minimum to maximum value. Rise time is usually measured from 10 % to 90 % of the pulse value. In contrast, fall time is the time it takes for the pulse to go from the highest value to the lowest value, measured from 90 % to 10 %.

Table 4.2: Specifications for PWM circuit generator signal rise/fall time on point VG

ID	SPECIFICATION	STANDARD	CHAPTER/POINT	DEVIATION ACCEPTED	CHARGING SIDE
15	Rise time (10 % to 90 %) in 2us (max)	IEC 61851-1 / SAEJ1772	A.3 - Table A.2 / 5.2 - Table 4	-	EVSE
16	Fall time (90 % to 10 %) in 2 us (max)	IEC 61851-1 / SAEJ1772	A.3 - Table A.2 / 5.2 - Table 4	-	EVSE

A transient analysis was conducted with a start and stop time specifically set to plot only one pulse on the simulation results 4.9. As this simulation requires great

detail once very small time intervals are being analyzed, a very short time step was chosen.

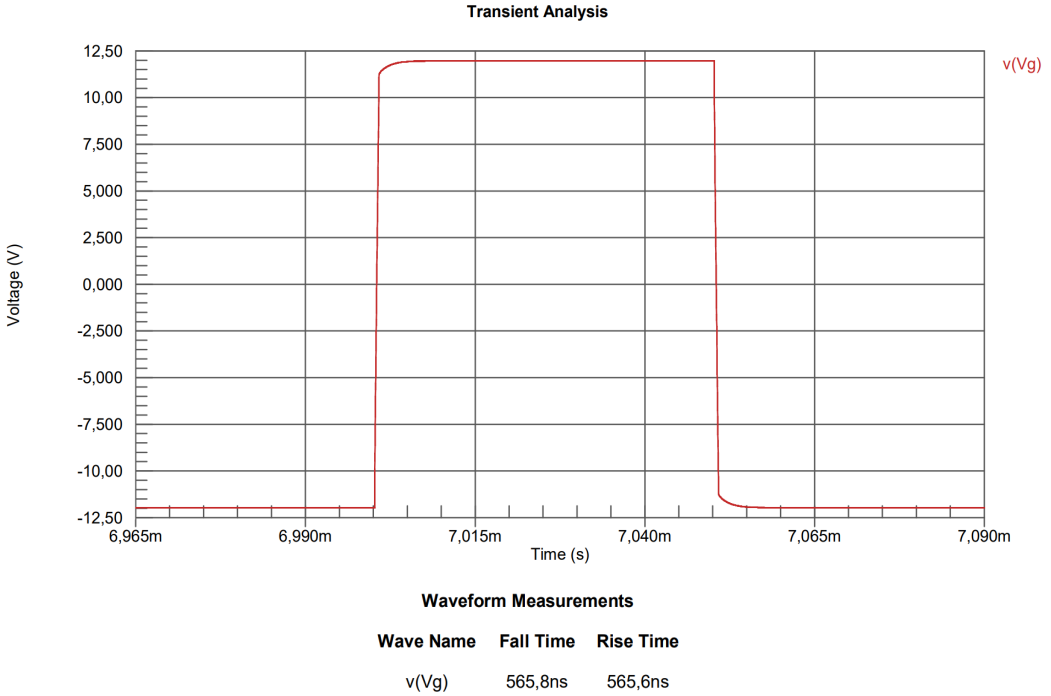


Figure 4.9: Transient simulation result on point Vg with rise and fall time measurements

Using the information presented in Figure 4.9, it can be observed that by utilizing the automatic Mixed Simulation feature, the rise and fall time of the signal edges can be calculated efficiently. This feature calculates the time intervals from 10 % to 90 % of the rising edge (and vice-versa of the falling edge) of the signal. It is worth noting that the calculated time intervals are well within the recommended maximums presented in table 4.2, indicating that requirements 15 and 16 have been met.

The IEC 61851-1 and SAEJ1772 standards require that the rise time from the beginning of the rising edge to 95 % of it (steady state) must be completed in under 3 μs (as shown in table 4.3). To check if this requirement is met, the waveform on Figure 4.9 was zoomed in, and measurements were taken using two cursors. Additionally, some simple calculations were necessary to determine the voltage value corresponding to 95 % of the rising edge signal.

Table 4.3: Specifications for PWM circuit generator signal rise/fall time on point VG

ID	SPECIFICATION	STANDARD	CHAPTER/POINT	DEVIATION ACCEPTED	CHARGING SIDE
17	Settling time to 95 % steady state in 3 us (max)	IEC 61851-1 / SAEJ1772	A.3 - Table A.2 / 5.2 - Table 4	-	EVSE

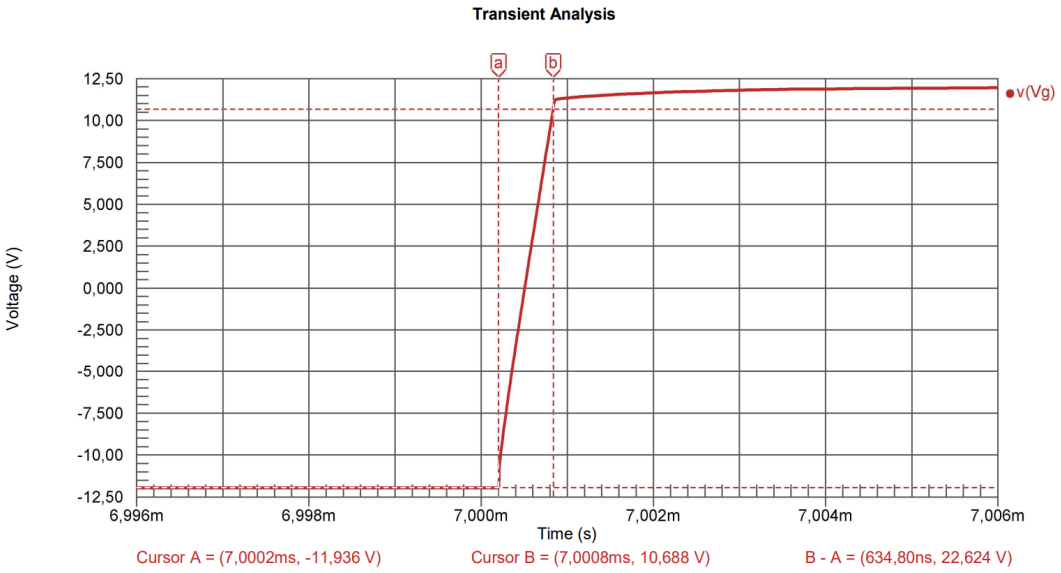


Figure 4.10: Transient simulation result on point Vg with cursors measuring Δt for 95 % of pulse edges rise time

It can be observed from the analysis in Figure 4.10 that the time required to transition from the negative steady state to 95 % of the rising edge is well within the stipulated 3 μs, given that tB - tA = 634.8 nS. Hence, specification 17 is also satisfied.

Voltage on point Va

Following, in table 4.4, it's possible to find additional project specifications. This table presents the requirements of the IEC 61851-1 and SAEJ1772 standards, which state the voltage level of each charging state and how both sides of the control pilot circuit must behave to achieve those states. For more information about the charging states, please refer to Chapter 2.

Table 4.4: CCS charging states specifications and both charging sides' necessary actions to create them

ID	SPECIFICATION	STANDARD	CHAPTER/POINT	DEVIATION ACCEPTED	CHARGING SIDE
3	EV responds by applying a resistive load to the positive half-wave to the control pilot circuit	IEC 61851-1	A.2.2	-	EV
4	The EVSE must be able to determine that the connector is inserted into the vehicle inlet and adequately connected to the EV by sensing resistance R3 as shown in Figure 1	SAEJ1772	5.3.1	-	EV
5	The EVSE is able to indicate to the EV/PHEV that it is ready to supply energy by turning on the oscillator and providing the square wave signal specified in Figure 1	SAEJ1772	5.3.2	-	EVSE
34	The EV supply equipment shall verify that the EV is properly connected by verifying the presence of the diode in the control pilot circuit, before energizing the system	IEC 61851-1	A.3	-	EVSE
35	State A - Va (voltage supply from SECC side on FIGUE A.1) should have trypical value of 12V if the EV is NOT connected to the EV supply equipment	IEC 61851-1 / SAEJ1772	Table A.4 / 5.2 - Table 3	11 to 13V	EVSE
36	State B - Va (voltage supply from SECC side on FIGUE A.1) should have trypical value of 9V if the EV is connected to the EV supply equipment and S2 is open (not ready to accept energy).	IEC 61851-1 / SAEJ1772	Table A.4 / 5.2 - Table 4	8 to 10V	EVSE
37	State C - Va (voltage supply from SECC side on FIGUE A.1) should have typical value of 6V if the EV is connected to the EV supply equipment and S2 is closed.	IEC 61851-1 / SAEJ1772	Table A.4 / 5.2 - Table 5	5 to 7V	EVSE

As shown in Figure 4.6, one software-activated switch (S2) is necessary to define state C (specification 37 on table 4.4). However, the schematic presented in Figure 4.11 shows three time-activated switches with the following purposes:

- **Switch 1:** this switch simulates the car being plugged;
- **Switch 2:** this switch simulates the software-controlled S2 on the EV side;
- **Switch 3:** this switch simulates the software-controlled PWM activation (or deactivation) by the MSE1021 chip.

The three switches are activated at three different short time intervals, which may not be an accurate representation of how things work in reality, where other timing and safety specifications are considered. However, for the purpose of this simulation, short intervals between states are used to study the behaviors of the circuit's pulse and voltage.

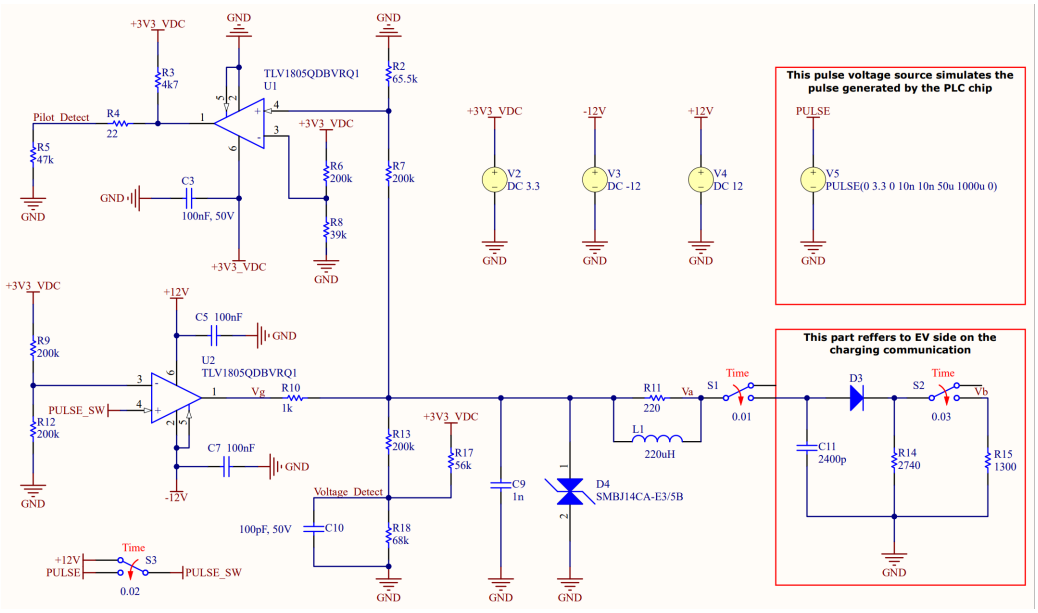


Figure 4.11: CP charging states simulation schematic

Running a transient analysis of the circuit presented in Figure 4.11 results in the graphic presented in Figure 4.12.

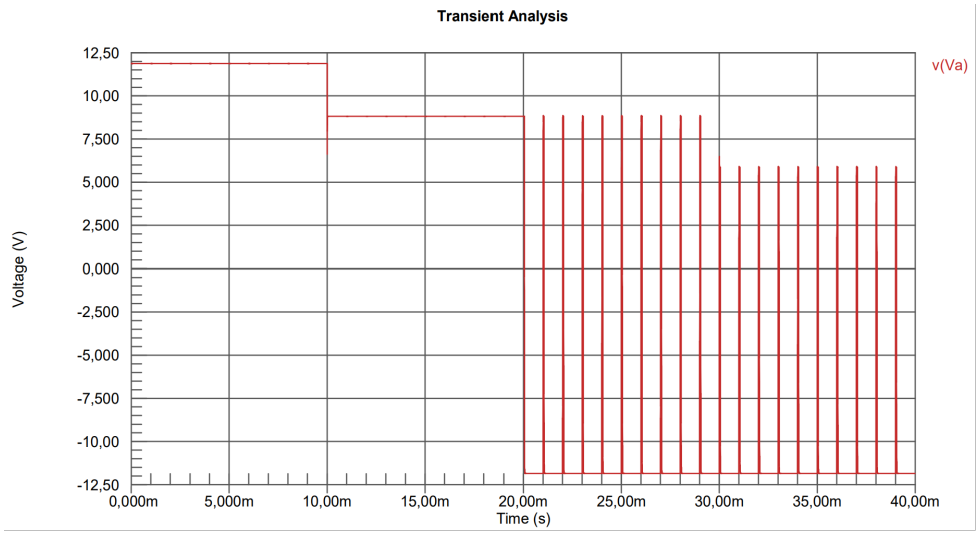


Figure 4.12: CCS charging states transient analysis of the circuit presented on Figure 4.11

Looking closely at Figure 4.12, it's apparent that:

- **Specification 35** is fulfilled, as within the first 10 ms, the voltage level at point Va is approximately 12 V (precisely 11.87 V), well within the accepted deviation specified;
- **Specifications 3, 4, and 36** are satisfied, as immediately after S1 closes at 0.01s, the voltage at point Va drops to around 9 V (precisely 8.82 V),

remaining within the specified deviation. This occurs due to the establishment of a voltage divider between R10 and R14 (as shown in Figure 4.11), with S2 open;

- **Specification 34** is met when the negative portion of the pulse at point Va is approximately -12 V. Even without diode D3 (as depicted in Figure 4.11), if S1 were connected directly to the R14 node, a voltage divider between R10 and R14 would still yield a negative voltage, as evidenced in Figure 4.13;
- **Specification 5** is fulfilled when, at 0.02s, upon the closure of S3, a square wave with a positive peak of 9 V (simulated as 8.82 V) and a negative baseline of -12 V (simulated as -11.86 V) is observed at point Va. This signifies the readiness of the EVSE to supply energy to the EV;
- **Specification 37** is met in the final 10 ms when the positive pulse voltage at point Va is approximately 6 V (precisely 5.86 V), remaining within the accepted deviation.

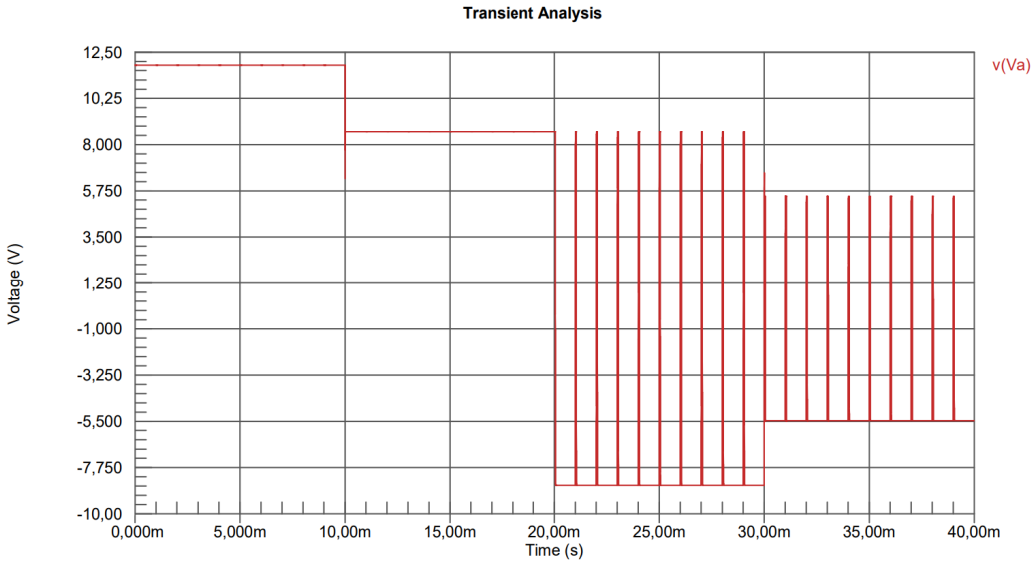


Figure 4.13: CCS charging states transient analysis of the circuit presented on Figure 4.11 without D3 present

To verify the functionality of the feedback circuits required by the MSE1021 chip, two additional DC sweep analyses are presented. The graphs' plots were bolded to differentiate the three signals. VertexCom documentation segments cannot be shared or cited due to confidentiality.

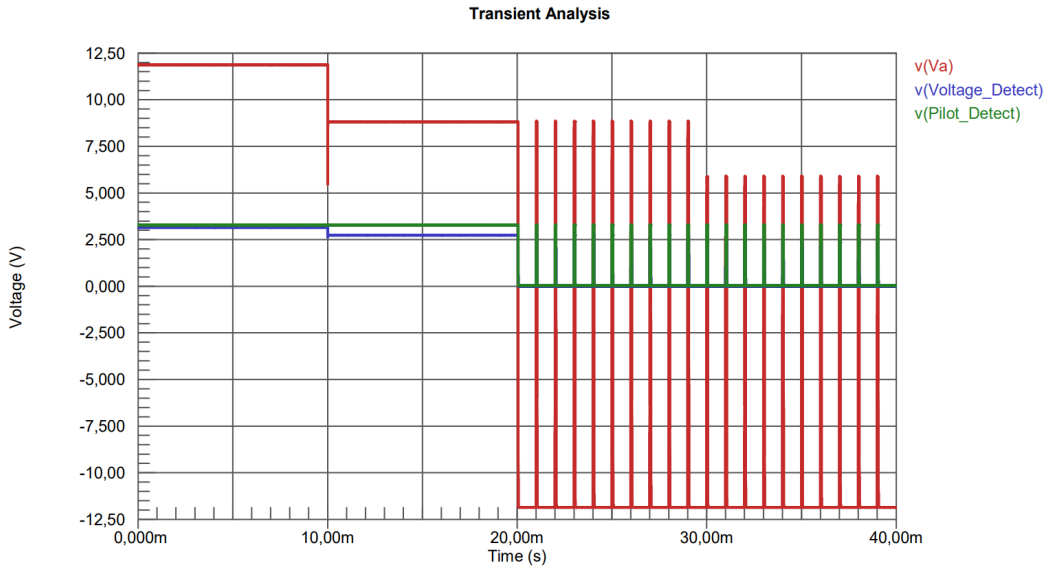


Figure 4.14: Transient analysis of Figure 4.12 plus CP circuit required feedbacks

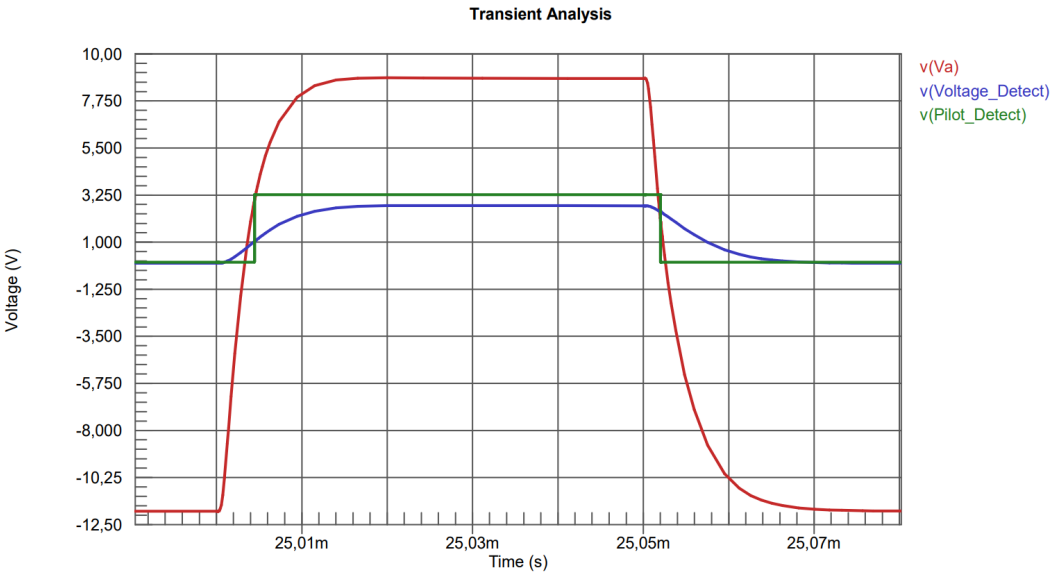


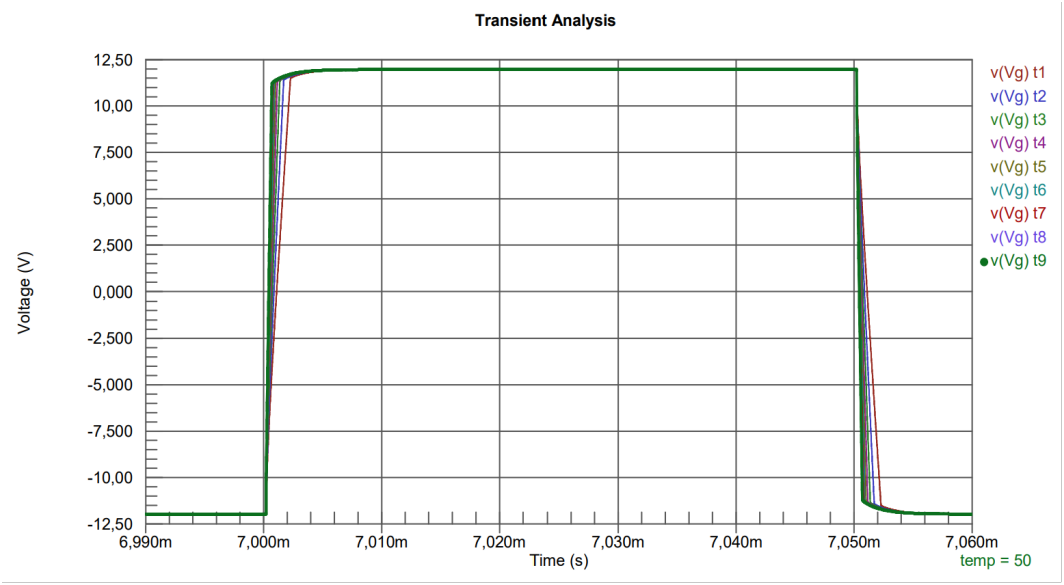
Figure 4.15: Zoom of Figure 4.14

It is evident from these two simulations that the feedback circuits are functioning properly. At the "Pilot_Detect" point, there is almost perfect pulse feedback, with the time interval between the edges of the feedback signal measuring approximately 47.5 μ. The pins receiving the frequency feedback achieve a precision of +/- 1 %, equivalent to +/- 10μs, meeting the specified tolerance. Additionally, the MSE1021 calculates the duty cycle by averaging multiple consecutive measurements. Consequently, the measured time interval between the feedback edges falls within the

specified range of 40 μs and 60 μs. At the "Voltage_Detect" point, it's also possible to view the desired proportional feedback wave of the Pulse signal at point Va, converted to values suitable for reading by an analog MSE1021 port.

Voltage on Point Vg - Temperature influence

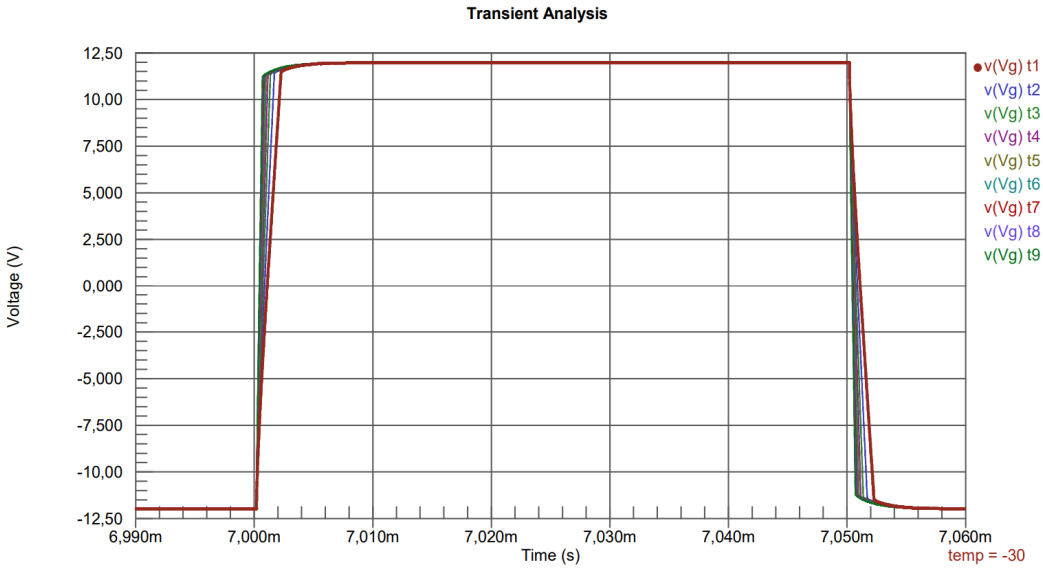
As stated in the i-charging Electric Vehicle Supply Equipment EVSE datasheets, the chargers must be capable of charging at temperatures ranging from -30 °C to 50 °C. The simulations presented below (Figures 4.16 and 4.17) demonstrate the effect of temperature on the voltage level on point Vg, with S1 open, and how they can affect the rising and falling times of the PWM signal.



Waveform Measurements

Wave Name	Base Line	Top Line	Fall Time	Rise Time
v(Vg)	-11,97 V	11,97 V	428,3ns	428,2ns

Figure 4.16: Transient simulation at 50 °C temperature sweep on point Va, including measurements of rise and fall times



Waveform Measurements

Wave Name	Base Line	Top Line	Fall Time	Rise Time
v(Vg)	-11,97 V	11,97 V	1,781us	1,781us

Figure 4.17: Transient simulation at -30 °C on point Va, including measurements of rise and fall times

With the increase in temperature ranging from -30ºC to 50ºC, it is observed that the times for the rising edge and falling edge either increase or decrease, consequently affecting the stabilization times. However, as evident in Figures 4.16 and 4.17 simulations measurements, at both -30 ° and 50 °, the timings specified by the standard for the rising and falling edges (10 % to 90 % and vice versa) are still met (2 μs maximum). To further explore the issue, additional simulations were carried out while excluding certain component families. Through this process, it was determined that capacitors had the greatest impact on the rising and falling edge times in the event of temperature variations.

It is also important to mention that, following some other analyses conducted on point Va, and considering the aforementioned simulations, it can be inferred that temperature changes do not have any impact on the voltage levels.

Voltage on Point Va - Monte Carlo Analyses

In this sub-subsection, Monte Carlo simulations are presented. These simulations allow varying tolerances of various circuit components and simulate multiple scenarios to analyze whether there is any combination where the circuit does not behave as desired. In this case, transient analysis on point Va was conducted in order to obtain the worst-case scenarios.

Table 4.5: Components tolerance values according to the respective datasheets (respectively [57] [58] [59])

Properties	Symbol	Test conditions	Value	Unit	Tol.
Capacitance accuracy	C	1 ±0.2 VRMS, 1 kHz ±10% @25 °C	0.1 - 100	nF	±10%
Voltage accuracy	V	5% - 100% load	3.3	V	±3%
Voltage accuracy	V	30% - 95% load	±12	V	±7%

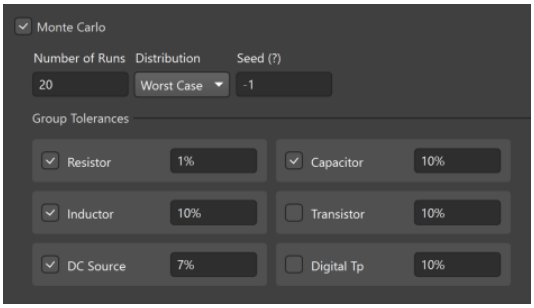


Figure 4.18: Monte Carlo setup on Altium Designer Mixed Simulation

The tolerances taken from each component datasheet are presented in Table 4.5 and those values were then used to fill in the Monte Carlo setup on Altium Designer Mixed Simulation (as shown in Figure 4.18). Besides the tolerances presented in the table, the standards recommend that all resistors in the PWM circuit have a tolerance of 1 %.

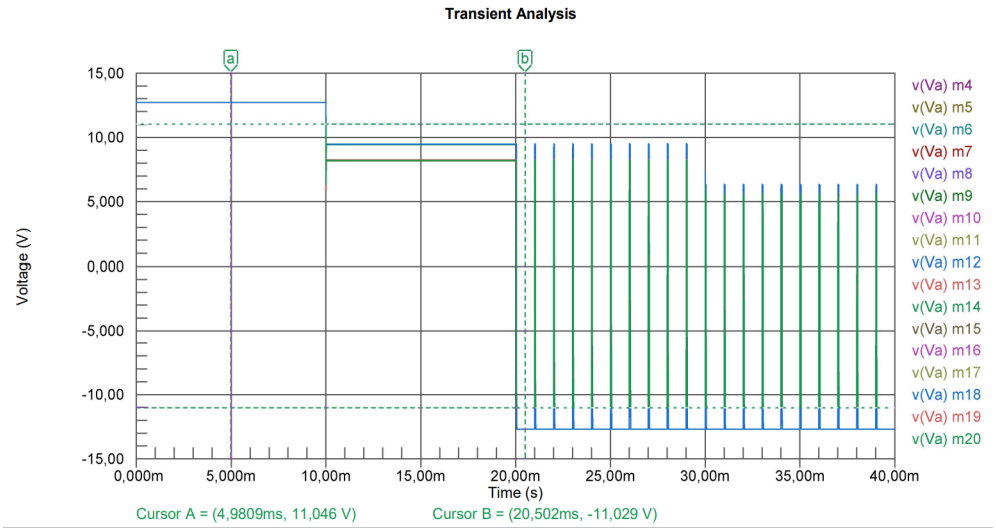


Figure 4.19: Worst case Monte Carlo analysis

Measurement Cursors

Cursor	Wave Name	X	Y
a	v(Va) m12	4,9809ms	12,709 V
b	v(Va) m12	20,502ms	-12,688 V

Measurement Cursors

Cursor	Wave Name	X	Y
a	v(Va) m20	4,9809ms	11,046 V
b	v(Va) m20	20,502ms	-11,029 V

Figure 4.20: Worst case Monte Carlo analysis measurements

After analyzing Figure 4.19 and 4.20, upon taking a deeper look into the Y measurements of the cursors for the two worst-case plots, it can be concluded that even on the plots created by the worst possible component variations within the tolerance values, the accepted deviation values of the circuit's voltage levels on point Va, as presented in Table 4.4 specifications, are still being met, despite being really close to those deviation values.

4.2.2 CAN Interface

The following subsection presents simulations of the CAN bus interface circuit. The typical application proposed by the LTC datasheet is presented in Figure 4.21 and shows the conventional point-to-point CAN bus link between two transceivers along with the twisted pair cable that helps to reduce electromagnetic radiation. The schematic in Figure 4.22 was designed to establish a point-to-point CAN connection, which can replicate a realistic future scenario. The red rectangles in the schematic denote the parts of the CAN interface that are not included in the project circuit but are required to create a real-life ambient simulation. The V1 voltage source replaces a CAN signal generated on the MCU. The CAN signal can be seen as a PWM signal with varying periods over time. In this case, as the purpose is simulating and analyzing the voltage levels on the CAN transmission data line, the signal's period is insignificant.

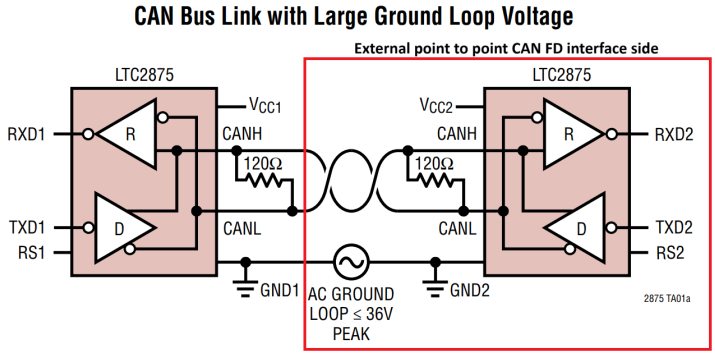


Figure 4.21: CAN Bus typical application presented on LTC2875 [51]

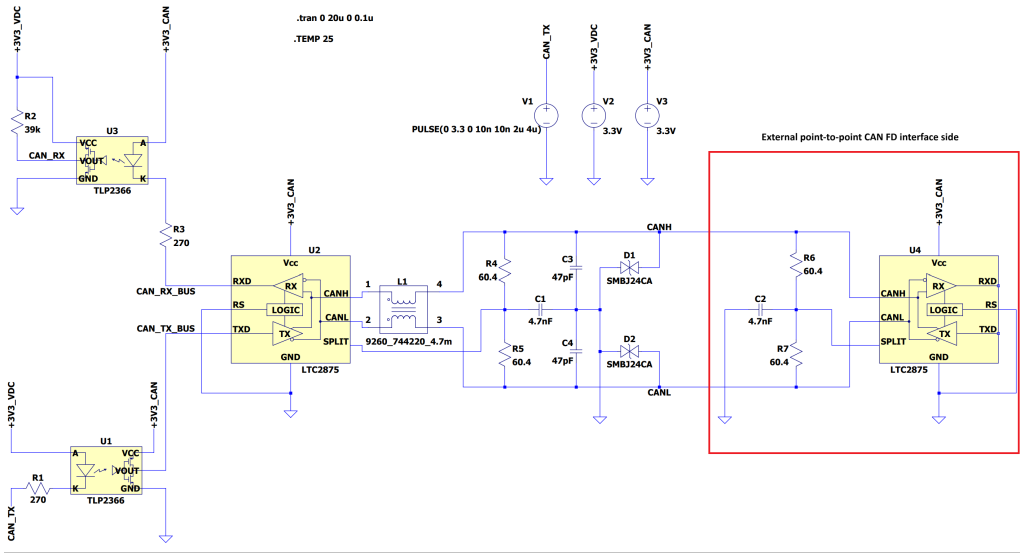


Figure 4.22: CAN Simulation Schematic on LTspice

Due to certain constraints, the simulation had to be performed on LTspice as the optocoupler's simulation model was only available in an encrypted format for LTspice and PSpice. Therefore, there was no sense in obtaining another simulator license, and the free software LTspice was employed to simulate the entire CAN interface. It's worth noting that the online SPICE model for the CAN transceiver with part number LTC2875 is not available. However, the transceiver has a pre-installed components library on LTspice, and a linked macromodel. A macromodel is a simpler circuit model consisting mainly of dependent and independent voltage and current sources, along with a few "real" elements. While macromodels do not provide a full transistor-level model, they can still offer a reasonably accurate first-order approximation of circuit performance in many applications. Even though it's not the most ideal simulation scenario, it's still the best one available [60].

As LTC2875 is ISO 11898-2 and Controller Area Network Flexible Data-Rate (CAN FD) compliant (consequently CAN 2.0 B compliant), the voltage and current levels of the data transmission lines meet the standards once they are imposed by the transceiver CANH and CANL pins. However, it's critical to measure and compare the data transmission line voltage values obtained through simulations with the transceiver driver voltage values on the datasheet to ensure no problems with the filter circuit. Therefore, the most critical analyses needed to be carried out were: transient analysis to understand how the circuit filters might affect the data transmission lines' voltage values; temperature sweep analysis to know if the data transmission lines' voltage levels can also be influenced by the way the filter circuit components behave with different temperatures; Monte Carlo analysis to understand the circuit behavior when oscillations to the circuit components and sources parameters occur, within their tolerance values; and finally, one of the most

critical analyses, the noise analysis, which differs from other analyses as it doesn't have a comparative basis on the datasheet due to the unknown nature of noise. The noise analysis helps to understand how the developed filter circuit attenuates the noise that might be present on the data transmission lines.

Transient Analysis

As mentioned before, the reference values for the data transmission lines voltage values are the transceiver driver voltage output values without load presented on the LTC2785 datasheet (table (4.6)) [51].

Table 4.6: LTC2875 driver voltage values [51]

Symbol	Parameter		Conditions	Min	Typ	Max	Units
$V_{O(D)}$	Bus Output Voltage (Dominant)	CANH	V_{CC} = 3.3V	2.15	2.9	3.3	V
		CANL	V_{CC} = 3.3V	0.5	0.9	1.65	V

To run a transient analysis, the following SPICE directive (Figure 4.23) needs to be applied to the CAN simulation schematic. This specific one creates a 20us transient analysis with a timestep of 0.1us, meaning that LTspice runs an operating point voltage every 0.1us, and the transient analysis plots and connects every one of those points, creating the waveform. In subsection 2.4, it was explained that increasing the step size results in a less detailed waveform, while decreasing it results in a more realistic representation of the waveform. For this reason, a step size of 0.1us was configured and the stop time was set to 20us in order to ensure that multiple states were captured and represented on the plot.

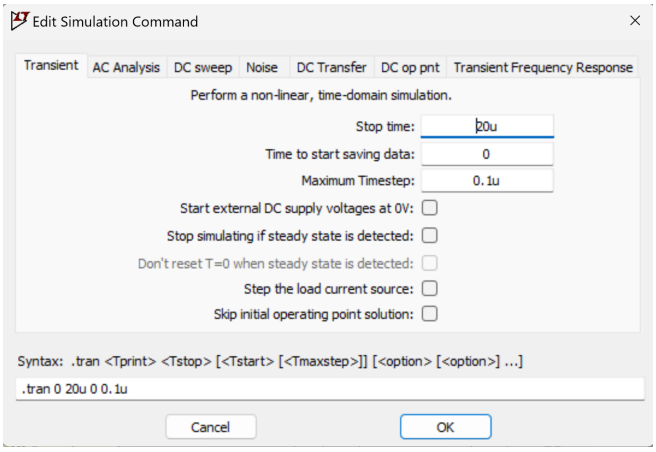


Figure 4.23: Simulation command editor to generate a transient analysis

The simulations were conducted under the following specifications: $T_A = 25$ °C, $V_{cc} = 3.3$ V and RL =120.8 Ω.

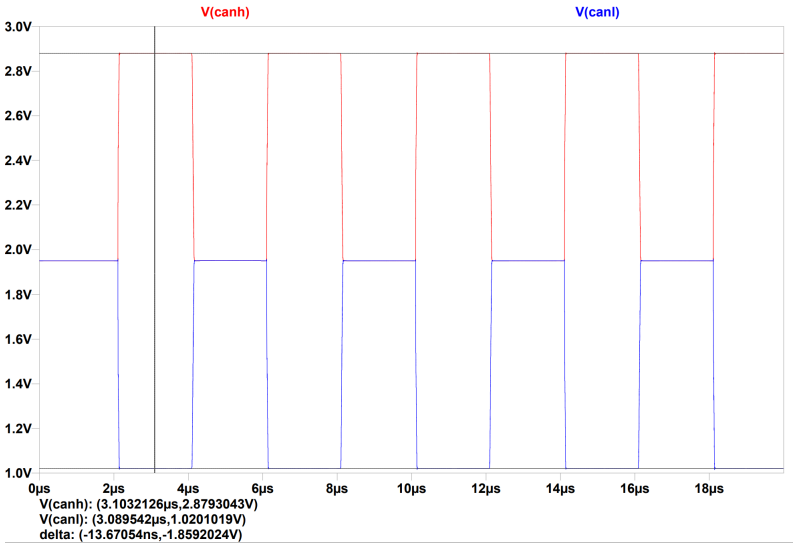


Figure 4.24: Transient Analysis with cursor placed on V(CANH) and V(CANL) waveforms during dominant state

It is possible to comprehend from Figure 4.24 that the voltage reading on CAN transmission data lines is 2.879 V for V(CANH) and 1.02 V for V(CANL) (the black lines represent the cursors used for reading these values). These voltage values fall within the datasheet value range (2.15 V $<$ 2.879 V $<$ 3.3 V for CANH and 0.5 V $<$ 1.02 V $<$ 1.65 V for CANL) as shown in Figure 4.21, and are almost identical to the typical values.

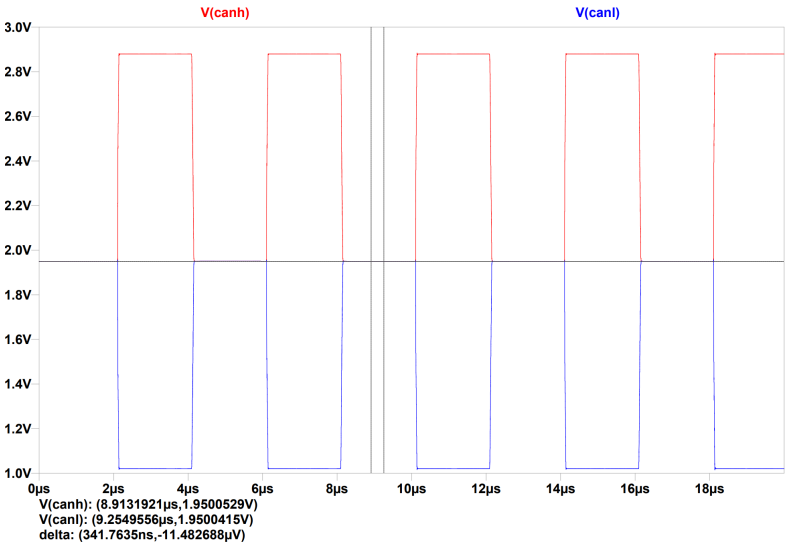


Figure 4.25: Transient Analysis with cursor placed on V(CANH) and V(CANL) wave forms during recessive state

It is possible to comprehend from Figure 4.25 that the voltage reading on CAN transmission data lines is 1.95 V for V(CANH) and V(CANL). These voltage values

fall within the datasheet value range (1.45 V < 1.95 V < 2.45 V for both lines) as shown in table 4.6, and are identical to the typical value.

In conclusion, it is possible to affirm that the filter circuit designed to reduce noise interference doesn't modify the voltage levels of the transmission data lines by comparing the values obtained from the latest simulations with those of the transceiver driver voltage output values without load. This means that the differential voltage value, which is the most crucial value, remains unaltered even after adding the filter circuit between the lines.

Temperature Sweep Analysis

As stated at i-charging Electric Vehicle Supply Equipment EVSE datasheets, the chargers must be capable of charging at temperatures ranging from -30 °C to 50 °C. The simulations presented below (figures 4.27 and 4.28) demonstrate the effect of temperature on CANH and CANL lines. Creating a transient analysis with two waveforms for the data lines transmission CANH and CANL is possible by including the following SPICE directive in the schematic (Figure 4.26). This analysis will show the behavior of these lines for a duration of 10us at two different temperatures, -30 °C and 50 °C, once the increment is 80 and the start value is -30.

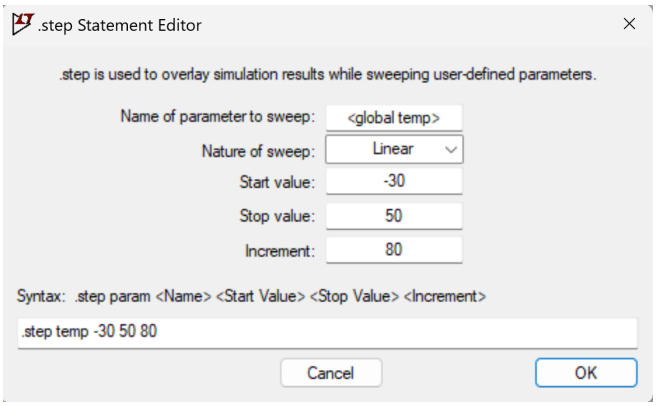


Figure 4.26: Step statement editor to create a temperature sweep

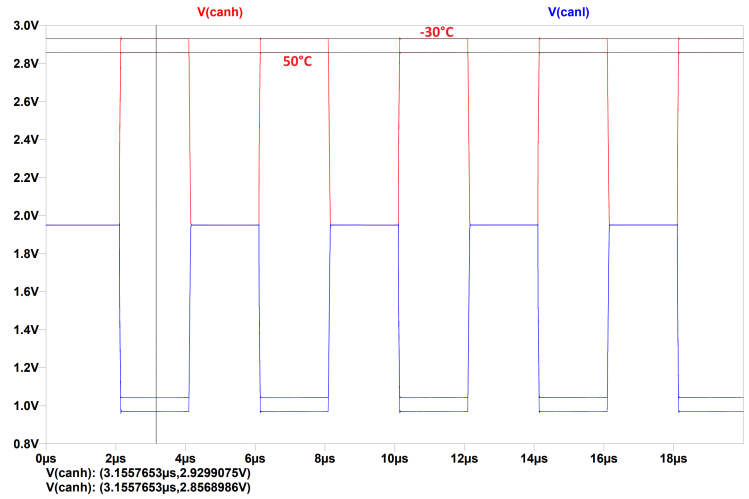


Figure 4.27: Transient Analysis with cursors placed on V(CANH) for T_A = -30 °C and T_A = 50 °C steps

In Figure 4.27, it's possible to understand that V(CANH) = 2.92 V when the temperature is -30 °C and V(CANH) = 2.85 V when the temperature is 50 °C. Compared with the values presented in Figure 4.21, the CAN High transmission data line voltage values for both temperatures are within the datasheet value range.

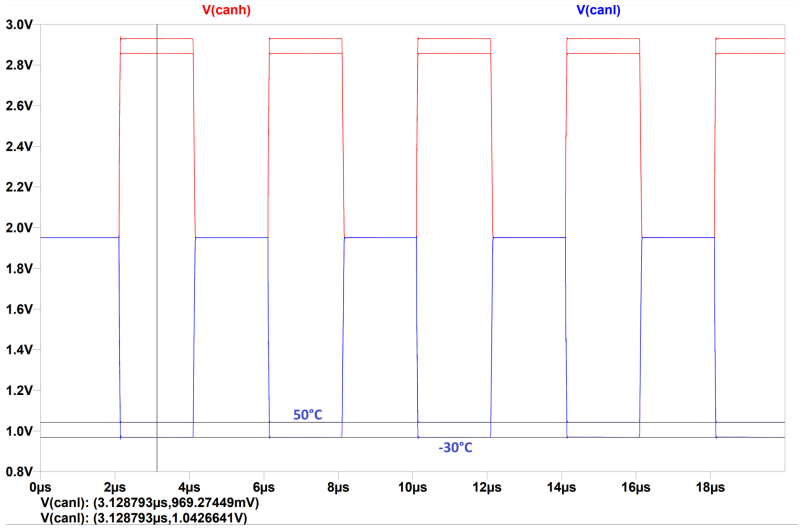


Figure 4.28: Transient Analysis with cursors placed on V(CANL) for T_A = -30 °C and T_A = 50 °C steps

In Figure 4.28, it's possible to understand that V(CANL) = 0.969 V when the temperature is -30 °C and V(CANL) = 1.04 V when the temperature is 50 °C. Compared with the values presented in Figure 4.21, the CAN Low transmission data line voltage values for both temperatures are within the datasheet value range.

It should be noted that the simulation macromodel of LTC2875 cannot be read, which makes it impossible to determine if the model has been designed to change

with temperature variations. However, based on the conclusion drawn from transient analysis that the filter circuit does not affect the data lines, it's theoretically possible to assume that the voltage levels can only be modified by the transceiver. This is because the transceiver's CANH and CANL pins control the line voltage levels. However, when the simulation results are compared with the $V_{OD(D)}$ (Output differential voltage of the driver in dominant mode) vs. temperature graph in the LTC2875 datasheet (Figure 4.29) [51], it becomes apparent that the macromodel varies with temperature. The simulations conducted for -30 °C show that $V_{OD(D)}$ is 1.95 V (2.92 V - 0.969 V), while for 50 °C, $V_{OD(D)}$ is 1.85 V (2.85 V - 1.04 V). These results are similar to the ones that can be read from the graph for V_{CC} = 3.3 V (Figure 4.29). Therefore, the capacitors and other components between the two data lines do not alter the voltage levels when the charging temperature is at its maximum and minimum.

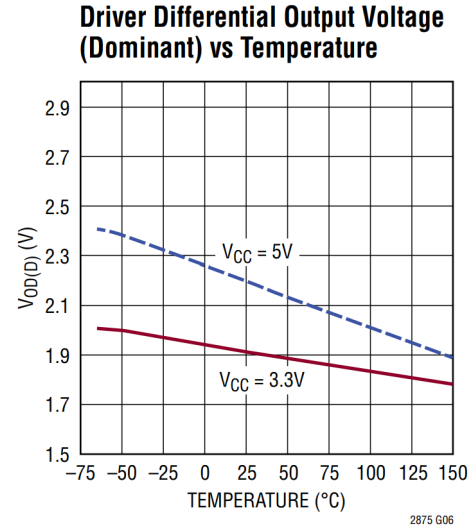


Figure 4.29: $V_{OD(D)}$ vs. Temperature graph in the LTC2875 datasheet [51]

Monte Carlo

Monte Carlo simulations demonstrate how circuit behaviors can be affected by adjusting the values of specific components within their tolerance limits. For instance, a resistor with a value of 200 Ω and a 1 % tolerance can have a value ranging from 198 Ω to 202 Ω. The tolerances of capacitors, resistors, and voltage sources in the circuit were adjusted as per their respective datasheets. The voltage sources' tolerances were modified to match those of the DC/DC converter used in the power circuit.

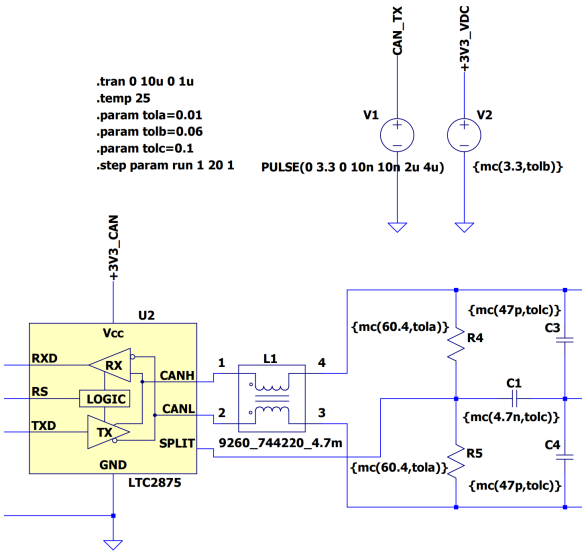


Figure 4.30: CAN simulation schematic segment that shows directives and components parts modeled with Monte Carlo distribution

Figure 4.30 displays a segment of the CAN simulation schematic that outlines how components should be modeled with Monte Carlo distribution and what directives are required to execute the Monte Carlo analysis.

For instance, the V2 voltage source has a nominal value of 3.3 V and a 6 % tolerance (*.param tolb = 0.06* defines the "tolerance b" variable as 0.06). The *tola, tolb*, and *tolc* are the tolerances of resistors, voltage sources, and capacitors, respectively. By defining *.step param run 1 20 1*, it's possible to generate a Monte Carlo distribution with 20 voltage states within the 6 % tolerance range. This distribution will run as many times as specified by the *run* parameter, thus producing a corresponding number of transient runs.

The following results were obtained after applying the directives presented and modeling every resistance, voltage source, and capacitor of the CAN simulation schematic with a Monte Carlo distribution.

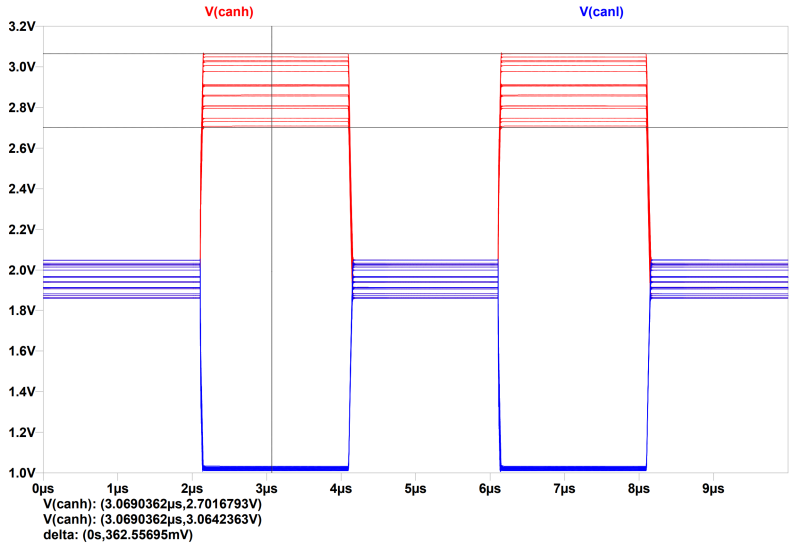


Figure 4.31: CANH highest and lowest voltage levels measurements on Transient Monte Carlo analysis during Dominant mode

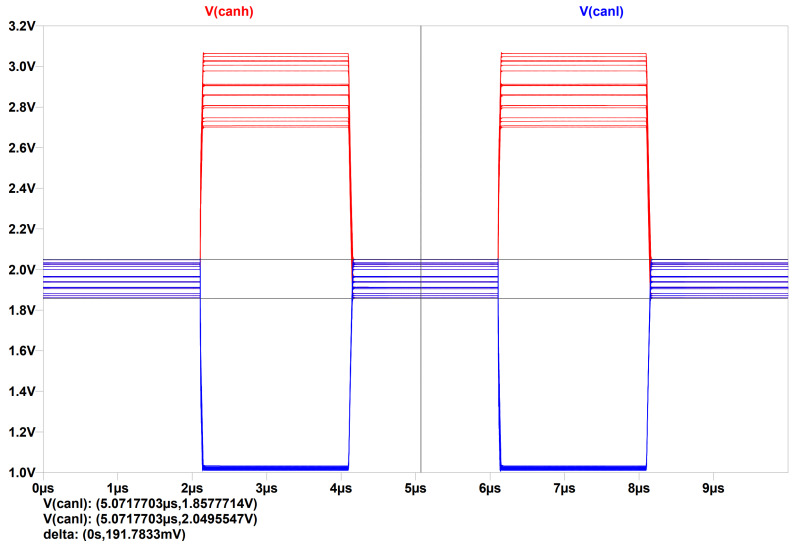


Figure 4.32: CANL highest and lowest voltage levels measurements on Transient Monte Carlo analysis during Recessive mode

Figures 4.31 and 4.32 show a transient analysis with 20 Monte Carlo distributions. The cursor measures the highest and lowest voltage levels of CANH during the Dominant mode and the highest and lowest voltage levels of CANL during the Recessive mode. It is worth noting that the CANL voltage levels do not change significantly during the Dominant mode, as it is the output of a Low Dropout Regulator (LDO) DC/DC converter whose Vin voltage is the VCC voltage. The maximum deviations of that value do not change the LDO output. On the other hand, the CANH voltage level also depends on an LDO voltage output. However, since it is a higher voltage, closer to the standard 3.3 V VCC value, and the latest also suffers

deviations within its range tolerance during the analysis, the CANH voltage mirrors those deviations.

In conclusion, based on the latest simulations, it is evident that even in the worst-case Monte Carlo distribution scenarios, where the voltage level of CANH is at its highest or lowest in Dominant mode, the readings are still within the permissible range allowed for CANH voltage level on the LTC2875 datasheet (Figure 4.21). This implies that even if the values of the CAN interface circuit components are at their maximum or minimum tolerances, the circuit will continue to operate effectively and perform its intended tasks.

Noise Analysis

The simulations presented in this sub-subsection explain the noise suppression circuit's positive impact on the CAN transmission data lines. Every simulation Figure in this sub-subsection results from transient analysis on the CAN simulation schematic with various modifications.

Figure 4.33 demonstrates noise injection into the transmission lines, specifically the CANH line, by adding a white noise voltage source. White noise is a type of random signal that has the same intensity across different frequencies, resulting in a constant power spectral density, and it is commonly used in signal processing [61]. In real life, this means that the CANH line would be affected by an external random interference. To evaluate the effect of the noise suppression circuit on the transmission data line, the initial stage is to exhibit the CAN simulation schematic without any noise suppression element, apart from the terminal resistances set at approximately 120 Ω each, on both ends of the transmission lines. This technique has been previously clarified in the document. Subsequently, the waveforms of CANH and CANL simulation results are exhibited (Figure 4.34).

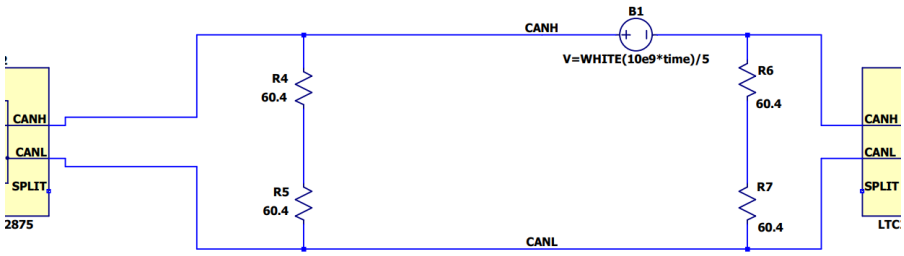


Figure 4.33: CAN bus circuit segment with a white noise voltage source added to CANH

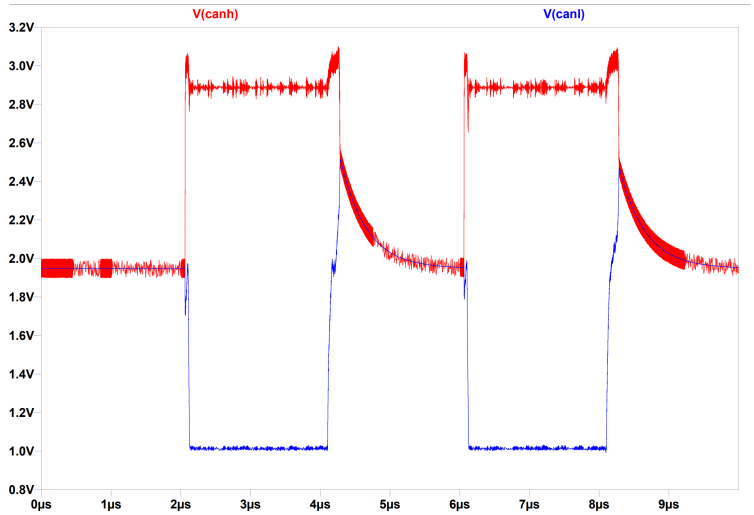


Figure 4.34: Transient simulation of the bus segment schematic presented on Figure 4.33

The waveforms' stability is affected during both dominant and recessive modes. During the recessive mode, it's notable that the voltage level takes a considerable amount of time to settle. Moving on, both CAN line waveforms are presented, this time with the split termination circuit included in the schematic.

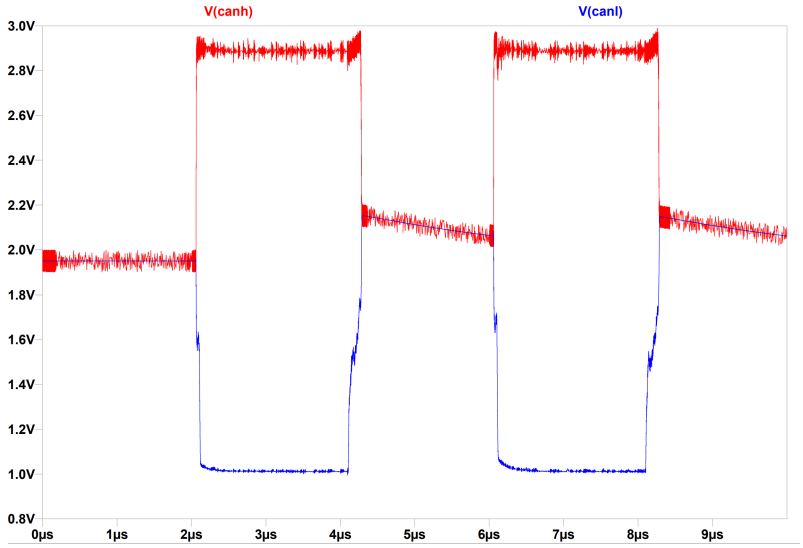


Figure 4.35: CANH and CANL waveforms with the split termination connection present on the circuit

Compared with the previous simulation (Figure 4.34), the voltage level during the recessive mode appears to be more stable.

Adding the common mode choke (Figure 4.36) right after the transceiver driver outputs, the CAN transmission line waveforms are:

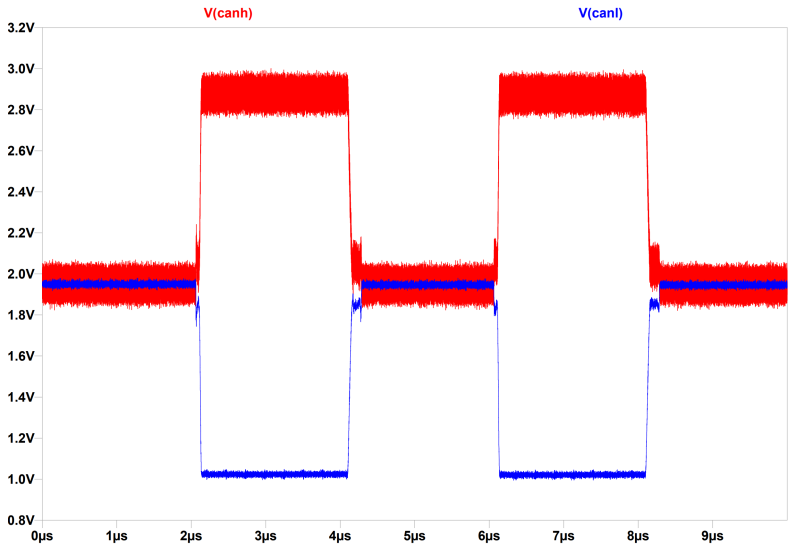


Figure 4.36: CANH and CANL waveforms with the split termination and CMK present on the circuit

Finally, capacitors are added to the circuit to reduce the amplitude of the noise on the CAN data lines.

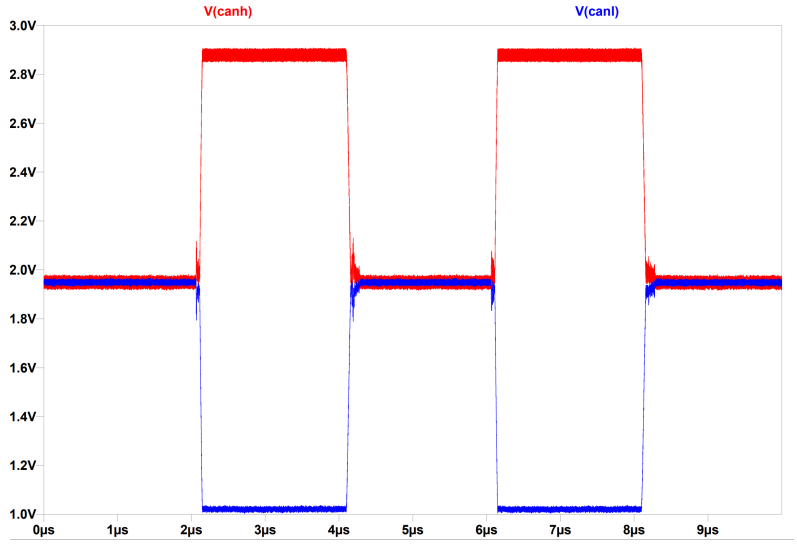


Figure 4.37: CANH and CANL waveforms with every component present on the suppression circuit

It is possible to analyze that the capacitors significantly reduce the noise amplitude. The noise attenuation on the CANH line, where the noise is injected, is more than 100 %. The noise suppression schematic, including all filtering components, is shown in Figure 4.38.

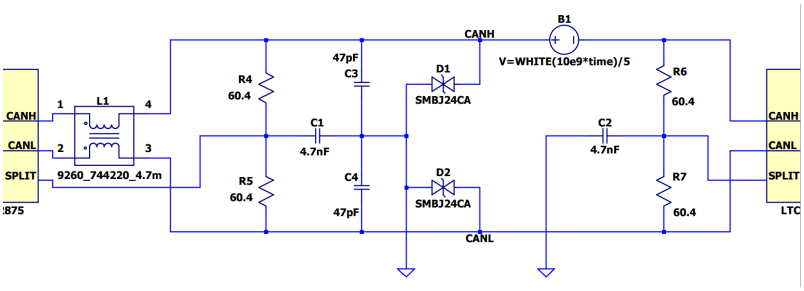


Figure 4.38: CAN bus segment of the simulation schematic with the presence of noise suppression circuit

Although no simulation was done to study the Transient-voltage-suppression (Transient-voltage-suppression (TVS)) diodes behavior, their purpose is to eliminate and drain any possible voltage spike to not damage the circuit.

This sub-subsection demonstrates and justifies the noise suppression circuit's purpose between the data lines, highlighting the significance of each circuit element individually. Considering that every simulation presented in this subsection demonstrates that the CAN bus circuit is well-designed, it is safe to affirm that the CAN bus interface circuit is ready for implementation.

4.2.3 Power Input Circuit

In the upcoming section, simulations of the power input filter of the board are presented. Two different DC sweep analyses were conducted to demonstrate the behavior and purpose of each component on the circuit. A new schematic was created solely for simulation purposes, which is shown in Figure 4.39. The 66 Ω resistor functions as a load and represents the entire maximum circuit's load when the maximum predicted current input, calculated earlier in this document, is approximately 364 mA. By applying Ohm's law, it is possible to calculate the resistor load that represents the full circuit load when the input voltage is 24 V: $R = \frac{U}{I} \equiv R = \frac{24}{0.364} \equiv R = 65.9 \approx 66\Omega$.

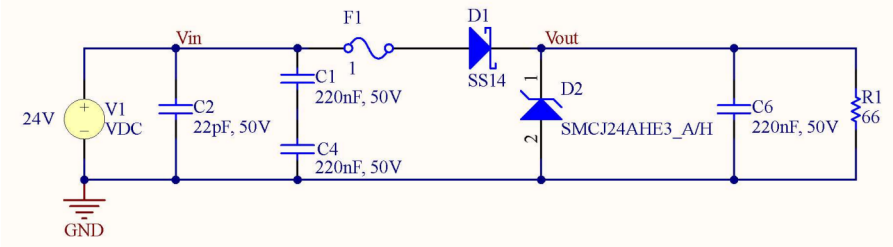


Figure 4.39: Power input simulation schematic

The major purpose of this circuit is to prevent the main circuit from:

- **Transient Voltages**, making use of one TVS diode (D2 on Figure 4.39). This diode starts conducting to the ground when the voltage exceeds 26.7 V.

Once the voltage level reaches 28.9 V (clamping voltage), the TVS diode fully conducts the transient current, stabilizing the voltage level at 28.9 V until the transient voltage ends.

- **Overvoltage and Overcurrent**, making use of a single TVS diode (D2) and a Positive Temperature Coefficient (PTC) resettable fuse (F1) (Figure 4.39) to prevent overcurrent faults. In the event of a short circuit or any event that causes the voltage and current levels to remain high for an extended period of time, the TVS diode conducts the excess power. In such a scenario, the PTC fuse will exceed its hold current of 0.5A at 20 °C and its trip current of 1A, acting like a high resistor to prevent overcurrent. This safeguards the circuit against overcurrent and overvoltage damage.
- **Reverse polarity**, making use of one schottky diode (D2 on Figure 4.39), because of it low forward voltage.

Two DC Sweep Analysis of this simulation schematic were conducted to understand whether the circuit would behave as predicted in real life.

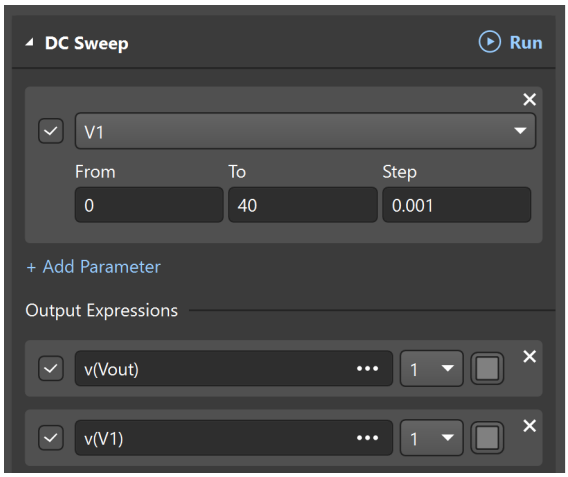


Figure 4.40: DC Sweep analysis setup on Mixed Simulation Altium Designer

The sweep analysis, set up to increment the voltage source value of Vin by 1mV from 0 V to 40 V, results in the waveforms plotted in Figure 4.41. The Figure displays the voltage values at the selected output points (as indicated in Figure 4.40) plotted against the swept input voltage (V1 source).

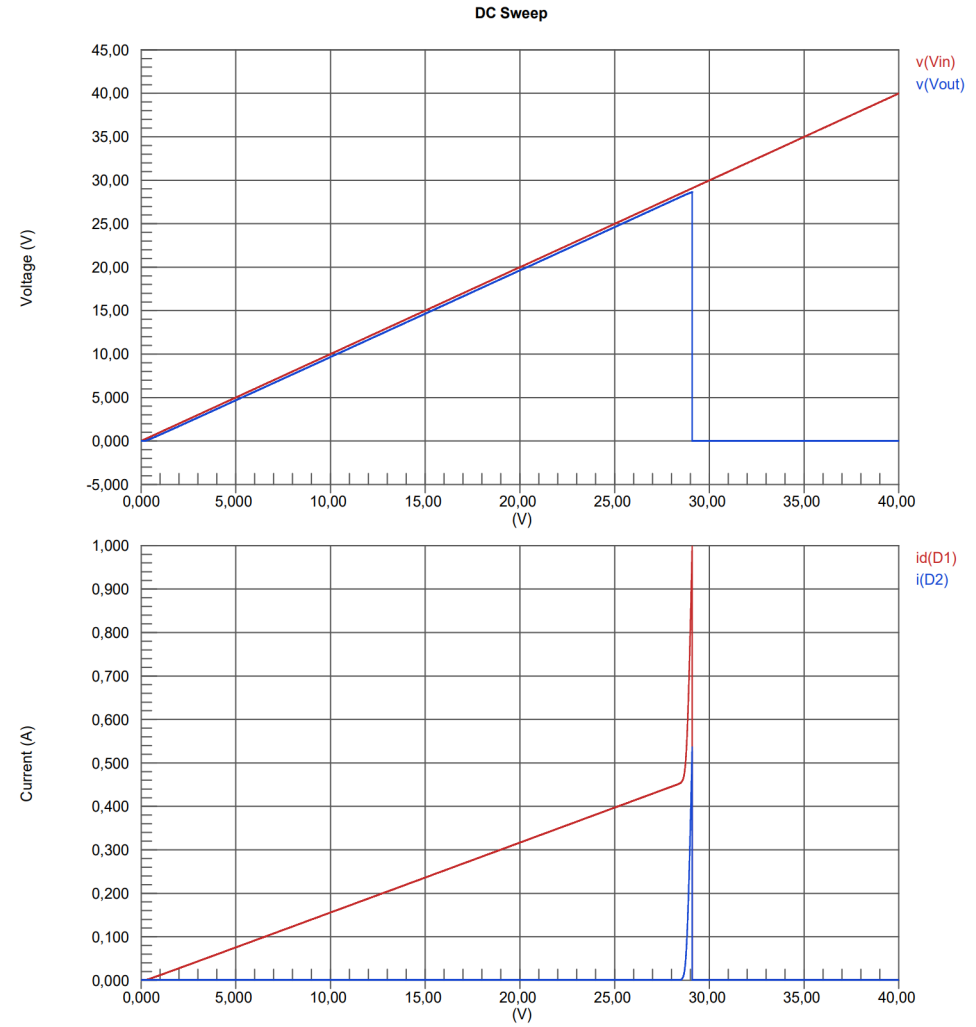


Figure 4.41: V(Vin) & V(Vout) VS Swept Input Voltage and I(D1)& I(D2) VS Swept Input Voltage

According to this analysis, the TVS functions as expected by causing a short circuit when the input voltage exceeds 26.7 V. This causes the voltage at Vout to drop to zero because, as previously mentioned and depicted in Figure 4.41, the PTC resettable fuse heats up due to the high amount of current flowing between Vin and the ground, causing it to become a very high-value resistor, not allowing any current to flow. As it's possible to observe in the Figure 4.41 waveforms, when the voltage input (Vin) exceeds 26.7 V, the behavior of D1 (Schottky) and D2 (TVS) is such that the TVS starts conducting the excess current, and the input current (I(D1)) quickly reaches 1A, which is the trip current value of the PTC resettable fuse. After this moment, if the voltage input value doesn't decrease, the PTC will cool down, and once it starts conducting again, the TVS will short the circuit again, causing the PTC to warm up and preventing any current from flowing. Unfortunately, this behavior cannot be observed in the simulations because it was not possible to find

any online spice model of the PTC resettable fuse, a simple fuse had to be used in its place. Once this fuse blows or melts, the only way to make the circuit work again is to replace the fuse. However, for simulation purposes, this type of fuse was used as it behaves almost the same as the PTC until the overcurrent occurs.

Chapter 5

Conclusions

With the project primary objective of developing a SECC schematic in compliance with specific standards and protocols, followed by validation through simulations, it is confirmed that this objective, along with the necessary preceding and subsequent objectives, has been successfully accomplished. The circuit schematic has been conceived in adherence to the specifications, and the following validation tests and simulations confirmed that all of these specifications have been met.

5.1 Final Remarks

The project provided a wealth of knowledge, not only in technical aspects but also in the field of electric mobility.

The experience at ISEP allowed for the application of acquired knowledge in practical scenarios, particularly in schematic design. This involved conducting datasheet consultations, performing calculations, and implementing auxiliary circuits.

Exposure to the industrial environment also led to the introduction of new concepts, such as vital rules in schematic design like protection circuits and filter circuits. Significant knowledge was also gained in the field of electric mobility, including insights into charging protocols and standards, and how a normal charging session is conducted. Moreover, proficiency in schematic design using the Altium Design Software and in circuit schematic simulation was achieved.

Throughout the project development, several challenges naturally surfaced, leading to deviations from the original schedule and considerable impacts on the project

options. The following setbacks are worth noting for their influence on the project's trajectory and pace.

PLC Chip Selection

During the selection phase of the 1^{st} PLC SoC option, a problem arose. After engaging in technical support correspondence and meetings with the chip manufacturers, it was determined that they could not provide the necessary support for the SECC circuit design development, as well as the future required assistance in developing the SECC firmware. As a result, an alternative HPGP chip had to be selected and adapted to the existing circuits designed at that time. This, naturally, caused a delay in the project.

Circuit Simulation

During the simulation phase, it was concluded that certain circuit blocks, previously earmarked for simulation, could not be simulated due to the unavailability of essential SPICE models for specific and critical components within those circuit segments. Consequently, the number of circuits amenable to simulation was reduced.

The overall experience has been exceedingly positive, leading to successful outcomes. All the objectives have been achieved, and substantial knowledge has been acquired as a result.

5.2 Future Work

In the context of future work, it is imperative to consider the following three main points:

- **PCB development:** this entails the design, production, and comprehensive testing of the PCB, including all hardware and communication interface evaluations;
- **Signal Integrity Simulation:** subsequent to the PCB design, It is crucial to perform signal integrity simulations in order to anticipate the possible effects of impedance mismatches, crosstalk, inductance, propagation delays, and other relevant factors on signal performance;
- **Firmware Implementation:** the final step involves the development, implementation, and rigorous testing of the necessary firmware to facilitate a charging session in compliance with all relevant communication and safety standards and protocols.

This project marked the initial phase towards the potential establishment of an in-home SECC. The realization of an in-home SECC is subject to the fulfillment of the three specified future objectives.

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Appendix A

Project Specifications

ID	SPECIFICATION	STANDARD	DEVIATION ACCEPTED
1	Control pilot must be able to set the duty cycle of a PWM signal or a continuous DC voltage signal	IEC 61851-1	
2	EV supply equipment may change the duty cycle of the PWM signal at any time	IEC 61851-1	
3	EV responds by applying a resistive load to the positive half-wave to the control pilot circuit	IEC 61851-1	-
4	The EVSE must be able to determine that the connector is inserted into the vehicle inlet and adequately connected to the EV by sensing resistance R3 as shown in Figure 1	SAEJ1772	-
5	The EVSE is able to indicate to the EV/PHEV that it is ready to supply energy by turning on the oscillator and providing the square wave signal specified in Figure 1	SAEJ1772	-
6	Functions, charge processe and states detected by control pilot should follow the sequences and functions presented	IEC 61851-1 / SAEJ1772	
7	Additional components required for signal coupling shall not deform the control pilot signal beyond the defined limits	IEC 61851-1	
8	Generator open circuit positive voltage should have typical value of 12V	IEC 61851-1 / SAEJ1772	11,4V to 12,6V
9	Generator open circuit negative voltage have typical value of -12V	IEC 61851-1 / SAEJ1773	-11,4V to -12,6V
10	Frequency generator output have typical value of 1000 Hz	IEC 61851-1 / SAEJ1774	980 us to 1020 Hz
11	Pulse width of 5% (50 us) for digital communication	IEC 61851-1 / SAEJ1772	45 us to 55 us (3% to 7%)
12	Duty cycle of 5% for indicating that digital communication is required and shall be established between the EV supply equipment and EV	IEC 61851-1	
13	Digital communication shall be established between the EV supply equipment and EV before enabling energy supply.	IEC 61851-1	
14	If digital communication cannot be established, the EV supply equipment shall: • stay in 5 % duty cycle or • change to x1 (100 % duty cycle) for at least 3 s or • change to x1 (100 % duty cycle) for at least 3 s and then change to a duty cycle between 10 % and 96 %.	IEC 61851-1 / SAEJ1772	
15	Rise time (10 % to 90 %) in 2us (max)	IEC 61851-1 / SAEJ1772	
16	Fall time (90 % to 10 %) in 2 us (max)	IEC 61851-1 / SAEJ1772	
17	Settling time to 95 % steady state in 3 us (max)	IEC 61851-1 / SAEJ1772	
18	Equivalent source resistance (R1) must be 1000 Ohm	IEC 61851-1 / SAEJ1772	970 to 1030 Ohm
19	EV supply equipment capacitance (Cs)	IEC 61851-1 / SAEJ1772	300 pF to 1600 pF
20	Cable capacitance (Cc) must have a maxiumum value of 1500 pF	IEC 61851-1 / SAEJ1772	
21	Optional series (damped) inductance 1 mH (max)	IEC 61851-1	
22	Permanent resistor value (R3) have a typical value of 2740 Ohm (State B)	IEC 61851-1 / SAEJ1772	2658 Ω to 2822 Ω
23	Switched resistor value for vehicles not requiring ventilation (R2) have a typical value of 2740 Ohm	IEC 61851-1	1261 Ω to 1339 Ω
24	Equivalent load resistance nominal value is 882 Ohm – State C	SAEJ1772	856 to 908 Ohm
25	Diode (D) voltage drop (2,75 – 10 mA, -40 °C to + 85 °C) have typical value of 0,7 V	IEC 61851-1 / SAEJ1772	0,55 V to 0,85 V
26	Reverse recovery time with maximum value of 200 ns	IEC 61851-1	

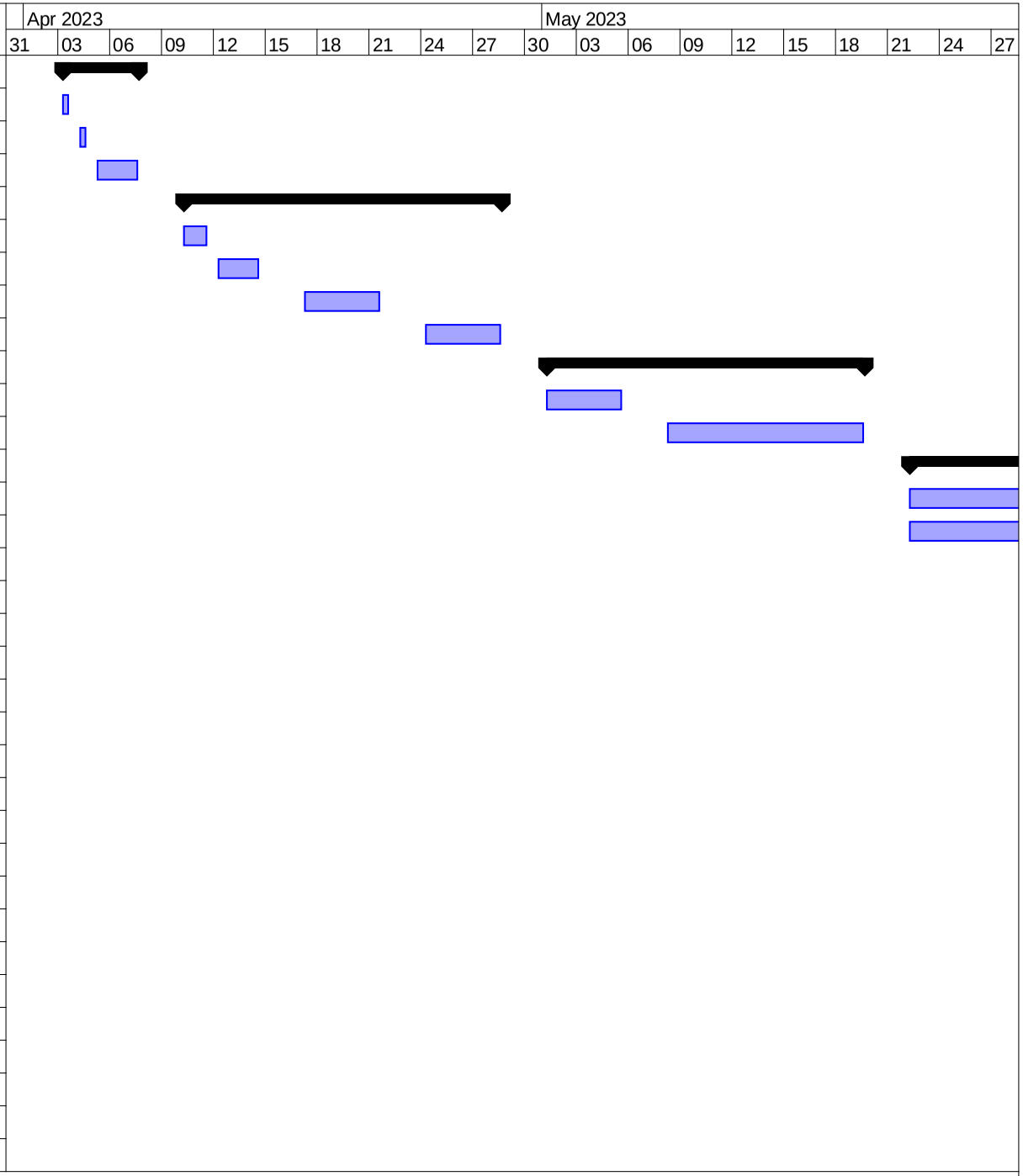
27	Total equivalent input capacitance with maximum value of 2400 pF	IEC 61851-1 / SAEJ1772	
28	Optional additional series (damped) inductance with maximum value fo 1 mH	IEC 61851-1	
29	Value ranges shall be maintained over full useful life and under design environmental conditions	IEC 61851-1	
30	1 % tolerance resistors are commonly recommended for this application	IEC 61851-1	
31	One state is only valid if it is within the values of Table A.4	IEC 61851-1	
32	It's not possible to have undefined voltage range, for the PWM signal, between the system states	IEC 61851-1	
33	The EV have do be capable of readind the voltage value (Vb) at any time	IEC 61851-1	
34	The EV supply equipment shall verify that the EV is properly connected by verifying the presence of the diode in the control pilot circuit, before energizing the system	IEC 61851-1	-
35	State A - Va (voltage supply from SECC side on FIGUE A.1) should have trypical value of 12V if the EV is NOT connected to the EV supply equipment	IEC 61851-1 / SAEJ1772	11 to 13V
36	State B - Va (voltage supply from SECC side on FIGUE A.1) should have trypical value of 9V if the EV is connected to the EV supply equipment and S2 is open (not ready to accept energy).	IEC 61851-1 / SAEJ1772	8 to 10V
37	State C - Va (voltage supply from SECC side on FIGUE A.1) should have typical value of 6V if the EV is connected to the EV supply equipment and S2 is closed.	IEC 61851-1 / SAEJ1772	5 to 7V
38	Low side of PWM signal should have typical value of -12V	IEC 61851-1	-13 to -11V
39	State E - Va (voltage supply from EVSE side on figure A.1) should have typical value of 0V if EVSE is disconnected, if utility power not available, or other EVSE problem	SAEJ1772	
40	The equipment grounding conductor must provide a return path for the control pilot current to insure that the EVSE equipment ground is safely connected to the EV vehicle chassis ground during charging. Loss of this signal shall result in the automatic de-energization at the EVSE.	SAEJ1772	
41	Input Voltage 24V	Internal	21,6 to 26,4V
42	Isolated supply voltage for CAN Circuit	Internal	
43	Isolated voltage supply for control pilot upper and lower threshold	Internal	
44	All DC/DC converters which are directly connected to the 24V source must be isolated	Internal	
45	State LED for main voltage values (24V directly connected DC/DC converters)	Internal	
46	Test points on every differential points right after DC/DC converters	Internal	
47	System must be equiped with na Homeplug GreenPHY SoC in order to establish digital communication with the EV	ISO 15118-3	
49	HPGP chip must have at least 1 SPI and 1 Ethernet interface	Internal	
50	Chip must have industrial grade qualification (-40 °C to 85 °C)	Internal	
52	System MPU frequency must be equal or superior to 800MHz	Internal	
53	System MPU must have SPI interface	Internal	
54	System MPU must have UART interface for debug purpouse	Internal	
55	System MPU must have at least one Ethernet interface	Internal	
56	System MPU must have SDMMC	Internal	

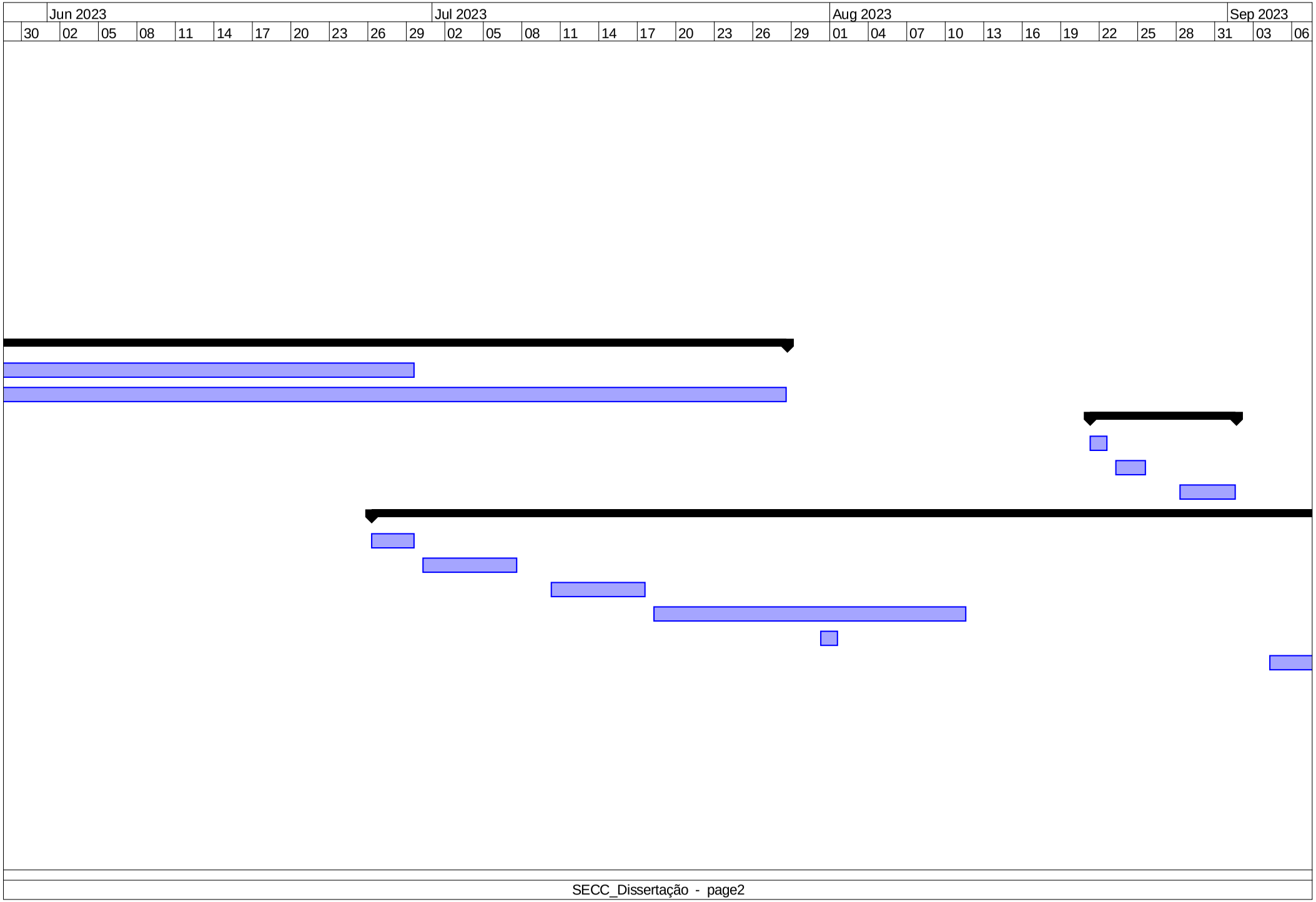
57	System MPU must have controller for external SDRAM supporting a minimum of 512 Mb	Internal	
58	MPU must have cryptography	Internal	
59	MPU must have 1 CAN interface	Internal	
60	System must be able to gennerate PWM functions used for low-level communication between the electric vehicle (EV) and the electric vehicle supply equipment (EVSE)	IEC 61851-1 / SAEJ1772	
61	System must have one state LED for indicating if there is power supply	Internal	
62	System must have one state LED for heartbeat (blinking)	Internal	
63	System must have one state LED for control pilot indicating: • OFF: state A/E/F • Blinking: state B • ON: state C	Internal	
64	System must have one state LED for PLC communication	Internal	
65	System must have 2 general purpouse state LED	Internal	
68	Operating system must be LINUX	Internal	
71	Develop SECC hardware considering future charger implementaion	Internal	
72	After its finalization, the hardware that has been developed should be prepared to implement the CCS standard.	Internal	
73	All components must respect industrial grade (-40 °C to 85 °C)	Internal	
74	CP circuit and measurements must be compliant with the standards that rule CCS charging communication	IEC 61851-1 & ISO 15118-3	
76	The board must have 3 RJ45 sockets with embedded LED for CAN and Ethernet	Internal	
77	The board must have 2 pin connector for input voltage	Internal	
78	The board must have a 2 pin connector for control pilot	Internal	

Appendix B

Expanded Gantt Chart

	Name
1	**Read initial documents**
2	Read IEC61851-1 standard
3	Read IEC61851-23 standard
4	Read CAN, Azure DevOps, and system architecture initial documents
5	**Research and study market options**
6	Research and read theses and patents within the same field
7	Research and study existing systems in the market
8	Research, study, and select the best options for the MCU
9	Research, study, and select the best options for the PLC chip
10	**Compare the available options for PLC chips and MCUs**
11	Comparing MCUs
12	Comparing PLC chips
13	**Hardware - Specifications and Topology**
14	High-level System Architecture
15	Specifications' definition and listing of necessary circuits and components
16	**Documentation**
17	Review the IEC 61851-1 standard
18	Create a document outlining the hardware requirements for the CP circuit
19	Update internal project specifications document
20	**Circuit's draft design**
21	Power circuit design
22	Design the electrical schematic of Lumissil's PLC chip (I/O and peripherals)
23	Design the electrical schematic of the MCU (I/O and peripherals)
24	Transition and adaptation of the project and circuit to the VertexCom chip
25	CAN electrical schematic design
26	CP electrical schematic design
27	Circuit finalization (review and some modifications)
28	**Schematics' design on dedicated software**
29	Adding and creating components in the library
30	Study, perception, and familiarization with the software
31	Power circuit design
32	Design the circuit for the VertexCom chip and peripherals
33	CP circuit design
34	PLC transformer circuit design

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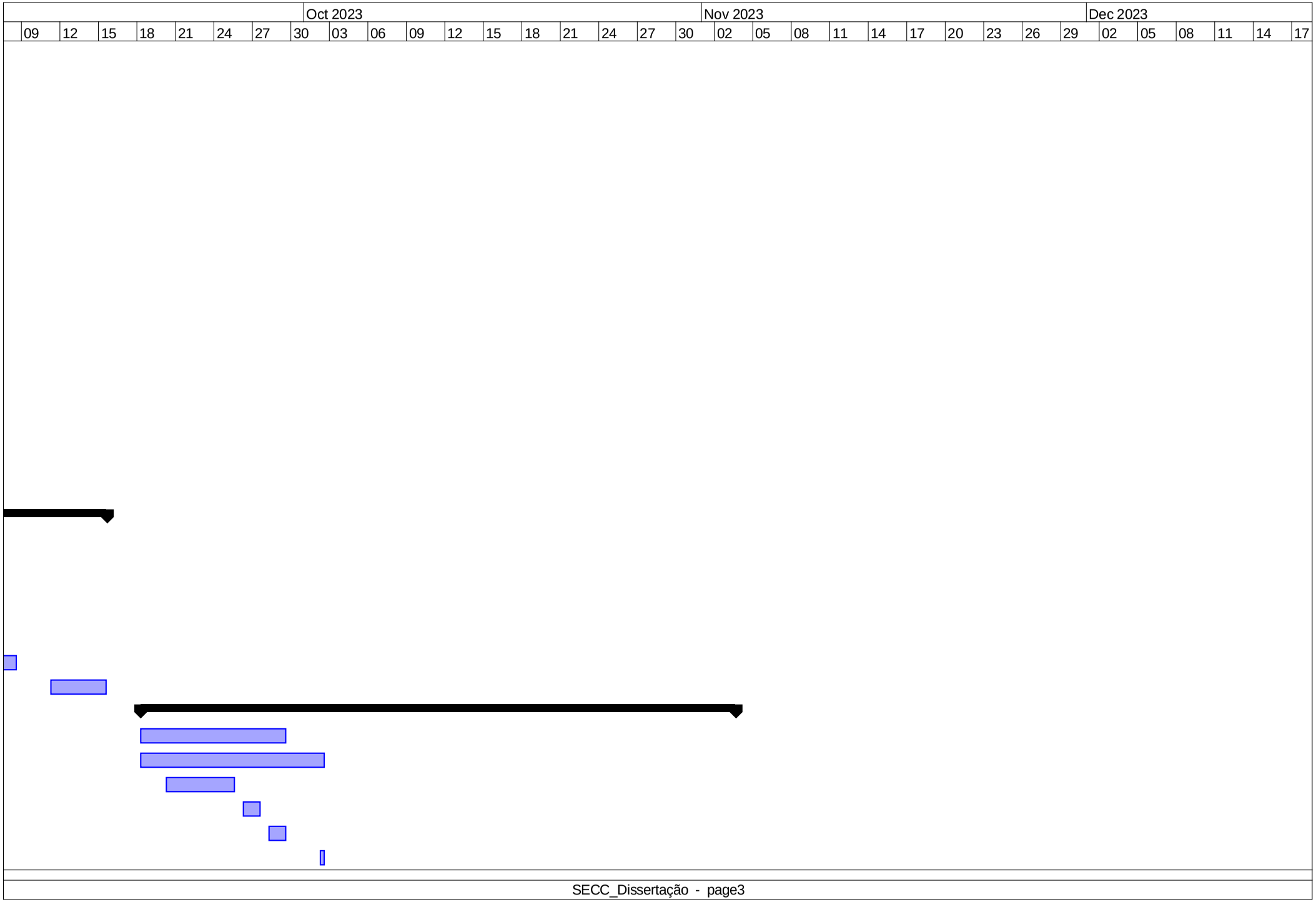
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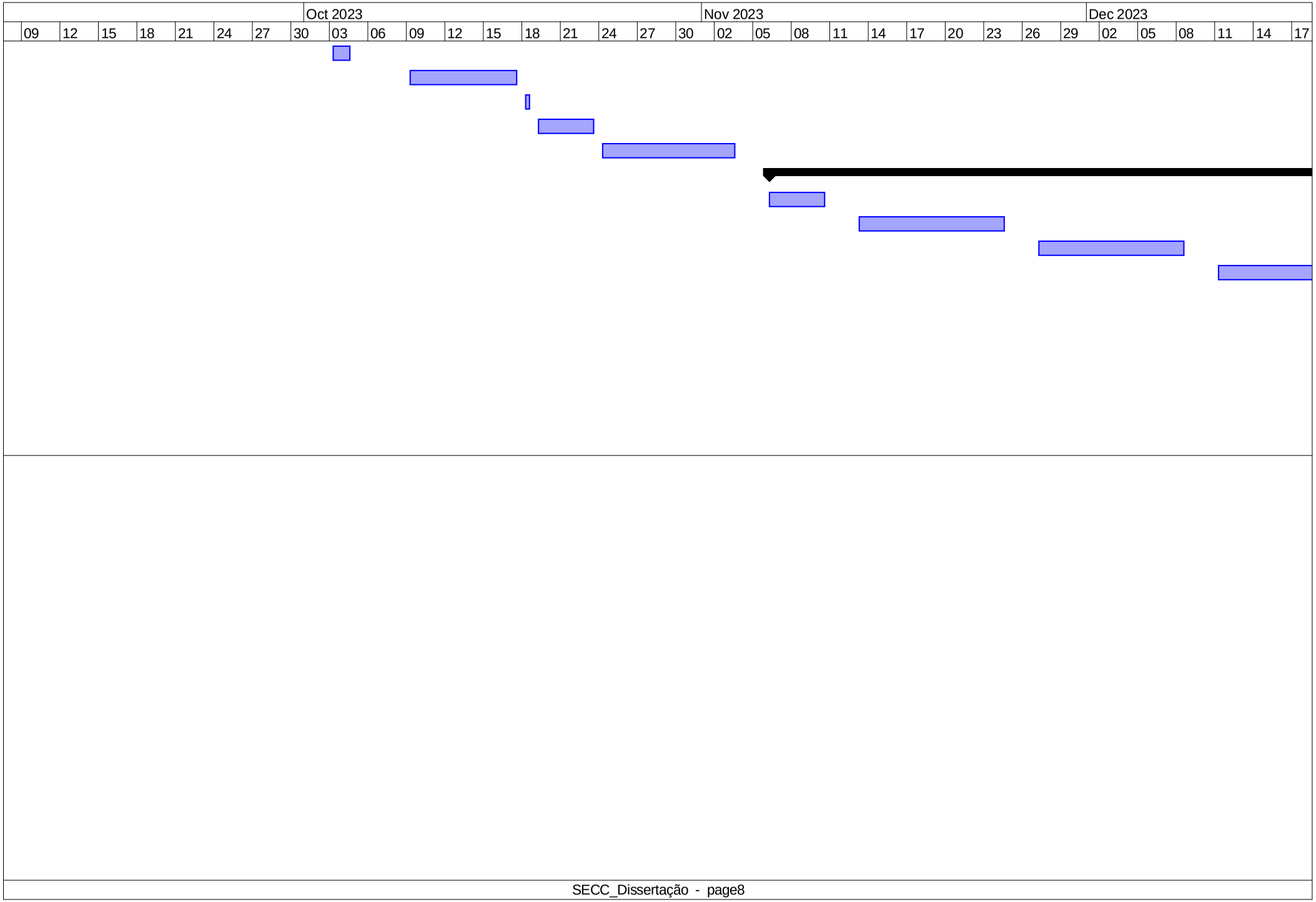
	Name	Apr 2023										May 2023									
		31	03	06	09	12	15	18	21	24	27	30	03	06	09	12	15	18	21	24	27
35	Comms circuit design																				
36	MCU and peripherals circuits design																				
37	Auxiliaries circuits design																				
38	Memories circuits design																				
39	Schematic conclusion and compilation																				
40	**Circuit schematics simulation**																				
41	Analyzing and comparing simulation software																				
42	Power schematic simulation																				
43	CAN schematic simulation																				
44	CP schematic simulation																				
45	Waveforms plots remake																				
46	**Thesis writing**																				
47	1st Chapter - Introduction																				
48	2nd Chapter - Technological Background																				
49	3rd Chapter - Implementation																				
50	4th Chapter - Debugging, Evaluation, Testing, Validation																				
51	5th Chapter - Final Conclusion																				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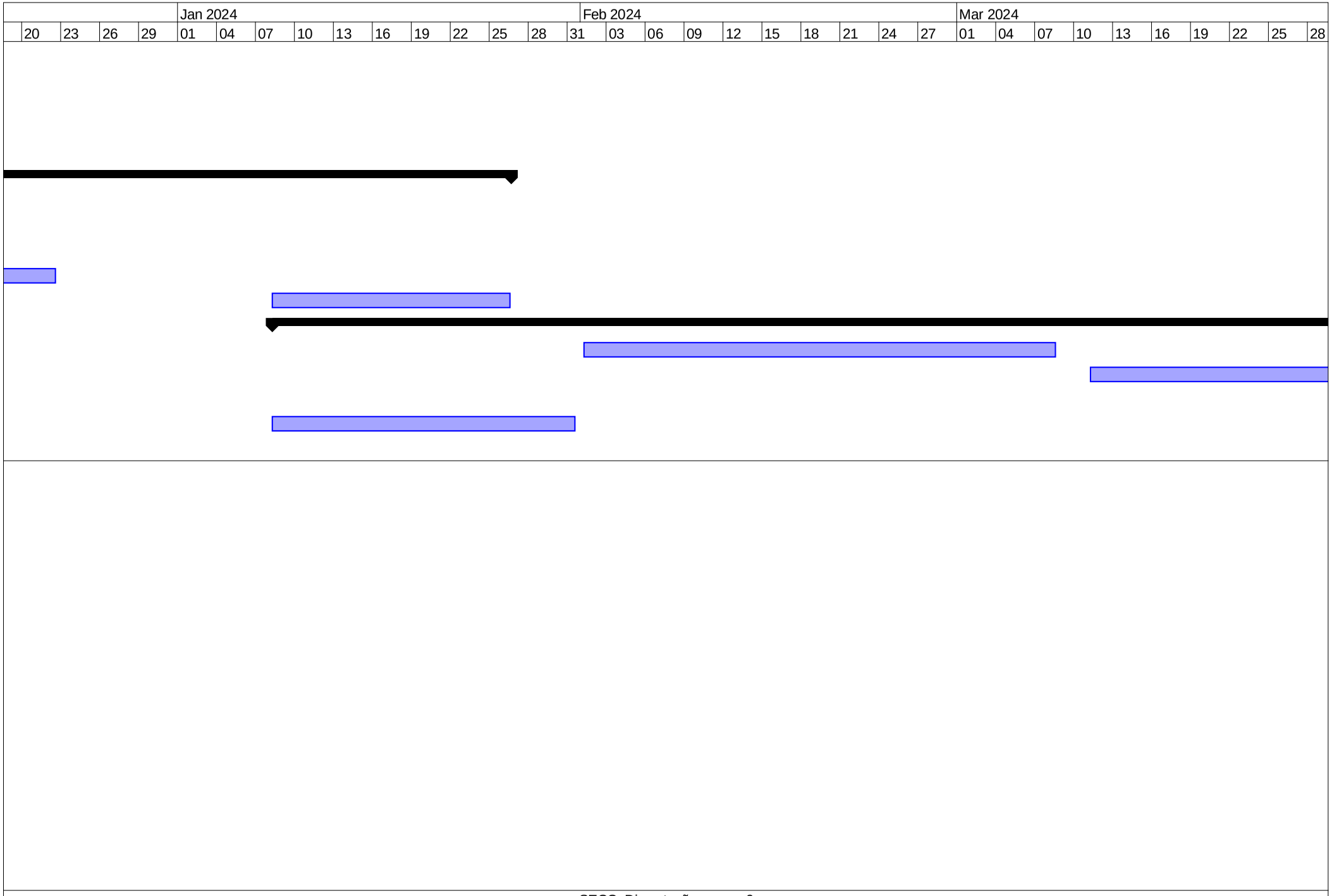
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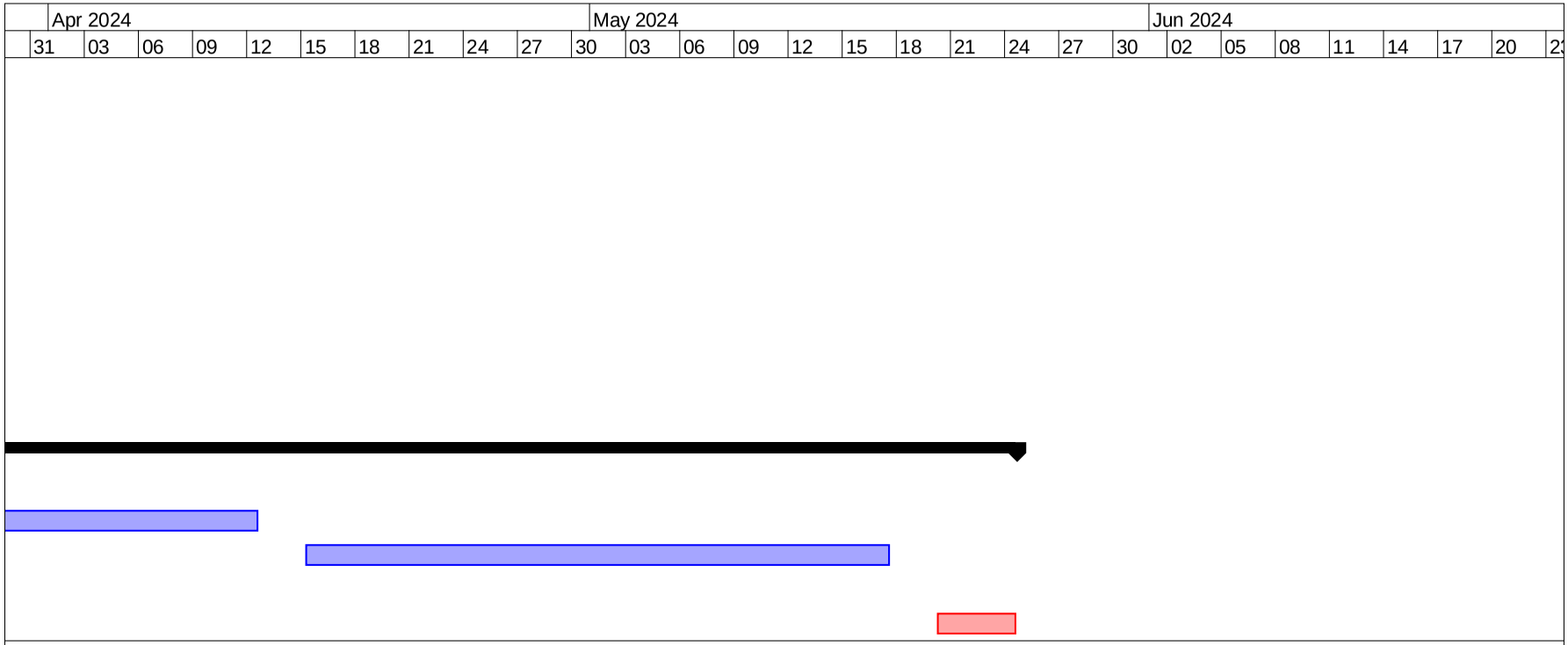
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Appendix C

MCU and PLC Chip Comparison Tables

C.1 MCU Comparison

The following pages present a detailed comparison table of the four MCU models initially considered for this project. The information pertaining to each cell was obtained from the official datasheets of the respective MCUs, namely the STM32MP153F [62], AM3352 [63], i.MX 6ULL [64], and ST2100 [62].

Note: This comparison is based solely on documents available online. Information may be limited or unavailable for certain features.				
Part Number	**STM32MP153F**	**AM3352**	**i.MX 6ULL**	**ST2100**
Manufacturer	ST	Texas Instruments	NXP	ST
Main Processor	• **Processor**: - 32-bit dual-core Arm® Cortex®-A7 800 MHz • **Cache:** - L1 32-Kbyte I / 32-Kbyte D for each core - 256 KB unified I/D L2 cache	• **Processor**: - 32-bit-core Arm® Cortex®-A8 1 GHz • **Cache**: - L1 32-Kbyte I / 32-Kbyte D - 256 KB unified I/D L2 cache	• **Processor**: - 32-bit dual-core Arm® Cortex®-A7 900 MHz • **Cache**: - L1 32-Kbyte I / 32-Kbyte D - 128 KB unified I/D L2 cache	• **Processor**: - ARM926EJ-S™ 32-bit RISC CPU up to 333 MHz • **Cache**: - L1 16-Kbyte I / 16-Kbyte D - 32 KB I TCM / 16 KB D TCM
Co-processor	Up to 209 MHz 32-bit Arm® Cortex®-M4 with FPU/MPU	-	NEON Media Processing Engine (MPE) Co-processor	-
External Memory Interfaces	• External DDR memory up to 1 Gbyte and 533 MHz clock - up to LPDDR2/LPDDR3-1066 16/32-bit - up to DDR3/DDR3L-1066 16/32-bit • Dual mode Quad-SPI memory interface • 3x SDMMC up to 8-bit • 16-bit SLC NAND with up to 8-bit ECC	• External DDR memory up to 1 Gbyte and 400 MHz clock - LPDDR, DDR2, DDR3, DDR3L 16-bit • Up to 7 chip select (NAND, NOR, Muxed-NOR, SRAM) with up to 16-bit ECC • 3x SDMMC up to 8-bit	• External DDR memory up to 1 Gbyte and 400 MHz clock - LPDDR, DDR2, DDR3, DDR3L 16-bit • 8-bit NAND with up to 40-bit ECC • 2x SDMMC up to 8-bit	• External DDR memory up to 333 MHz clock - DDR/DDR2 up to 16-bit; • 8/16-bit NAND/NOR flash
On-chip memories	• 384 Kbytes General-Purpose RAM Memory • 128 Kbytes ROM	• 64 Kbytes General-Purpose RAM Memory • 176KB of On-Chip Boot ROM	• 128 KB OCRAM • 96 Kbyte Boot ROM	• 8 Kbyte on-chip SRAM • 48 Kbyte on-chip boot ROM
Cryptography	Yes	Yes	Yes	Yes
Conectivity	• 6 × I2C FM • 4 × UART + 4 × USART • 6 × SPI • 3 × SDMMC up to 8-bit (SD / e•MMC™ / SDIO) • 2 × CAN • 2 × USB 2.0 high-speed Host + 1 × USB 2.0 full-speed OTG simultaneously – or 1 × USB 2.0 high-speed Host + 1 × USB 2.0 high-speed OTG simultaneously • 10/100M or Gigabit Ethernet GMAC (IEEE 1588v2 hardware, MII/RMII/GMII/RGMII) • Up to 176 GPIO's	• 3x I2C Master and Slave Interfaces • 6x UARTs • 2x Master and Slave McSPI Serial Interfaces • 3x MMC, SD, SDIO Ports • 2x CAN Ports (Version 2 Parts A and B) • 2x USB 2.0 High-Speed DRD • Up to Two Industrial Gigabit Ethernet MACs (10, 100, 1000 Mbps) • Up to 128 GPIO's	• 4x I2C, supports 400 kbps • 8x UARTs, up to 5.0 Mbps • 4x eCSPI (Enhanced CSPI), up to 52 Mbps each • 2x MMC/SD/SDIO card ports all supporting: • 2x CAN • 2x High-Speed (HS) USB 2.0 OTG (up to 480 Mbit/s) • Dual-megabit Ethernet controller, 10/100 Mbit/s	• I2C master/slave mode • 2x independent UARTs supporting hardware (HW) flow control • Master / Slave SSI • 2x independent “Controller Area Network” (CAN) interfaces compliant with CAN protocol version 2.0 parts A and B (up to 1 Mbit/s). • USB 2.0 (high-full-low speed) port with an integrated PHY able to work as a host or device • PCI Express and S-ATA • Up to 40 GPIO's
Power modes	• Run mode • Stop mode • LP-Stop and LPLV-Stop • Standby	• Active • Standby • Deepsleep0 • Deepsleep1 • RTC-Only	• RUN Mode • Low Power Mode • RTC-Only • OFF Mode	-
ADC	• 2 × ADCs with 16-bit max. resolution (12 bits up to 4.5 Msps, 14 bits up to 4 Msps, 16 bits up to 3.6 Msps) • Each ADC shares up to 20 external channels	• 12-Bit Successive Approximation Register (SAR) ADC with 200K Samples per Second	• 2 × 12-bit Analog to Digital Converters (ADC) with up to 10 input channels in total (12-bit resolution up to 1Ms/s sampling rate)	-
Clocks	• Internal oscillators: 64 MHz HSI oscillator, 4 MHz CSI oscillator, 32 kHz LSI oscillator • External oscillators: 8-48 MHz HSE oscillator, 32.768 kHz LSE oscillator • 5 × PLLs with fractional mode	• Internal 32 kHz Oscillator • External oscillators: 32K oscillator (CLK_32K_RTC), 19.2-MHz, 24-MHz, 25-MHz, or 26-MHz oscillator (CLK_M_OSC) • 5x ADPLLs to Generate System Clocks	• Internal oscillators: 40 kHz oscillator, • External oscillators: 24 MHz XTALI Oscillator, 32.768 kHz RTC_XTALI oscillator • 6 × PLLs	• External circuit for 24 MHz for MAster clock • External clock for 32,768 MHz RTC clock

Timers	• 2 × 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input • 2 × 16-bit advanced motor control timers • 10 × 16-bit general-purpose timers (including 2 basic timers without PWM) • 5 × 16-bit low-power timers • RTC with sub-second accuracy and hardware calendar • 2 × 4 Cortex®-A7 system timers (secure, non-secure, virtual, hypervisor) • 1 × SysTick M4 timer • 3x watchdogs	• 3x 32-Bit Capture Inputs or 3x Auxiliary PWM Outputs • 3x Enhanced High-Resolution PWM Modules • 3x 32-Bit Enhanced Quadrature Encoder Pulse (eQEP) Modules • 1x watchdog timmer	• 2 × 32-bit Enhanced Periodic Interrupt Timer • 2 × 32-bit General Purpouse timer • 16-bit counter PWM - 16-bit resolution and 4 x 16 data FIFO • 3x watchdog timmer	• 3x 16-bit general purpose timers with programmable 8-bit prescaler • Up to 4 GPIOs supporting PWM • Up to 4 GPIOs supporting double PWM. • 1x watch dog
Packages	• TFBGA 361 12x12x1.2 P 0.5 mm • LFBGA 354 16x16x1.7 P 0.8 mm • LFBGA 448 18x18x1.7 P 0.8 mm • TFBGA 257 10x10x1.2 P 0.5 mm	• 298-Pin S-PBGA-N298 Via Channel Package (ZCE Suffix), 0.65-mm Ball Pitch • 324-Pin S-PBGA-N324 Package (ZCZ Suffix), 0.80-mm Ball Pitch	• MAPBGA 14 x 14 mm, 0.8 mm pitch 289 balls • MAPBGA 9 x 9 mm, 0.5 mm pitch 272 balls	• FBGA 12 x 12 x 1.2 mm, pitch 0.5 mm
Availability, pricing, and suppliers	• Anglialive (official distrubutor) • In stock (21/03/2024) • Min. order - 1 uni • Price - 14.20€ Other vendors may offer the same product with different prices and higher minimum orders	• Texas instruments • In stock (21/03/2024) • Min. order - 1 uni • Price - 9,53€ Other vendors may offer the same product with different prices and higher minimum orders	• Rochester Eletronics • In stock (21/03/2024) • Min. order - 1 uni • Price - 10.34€ Other vendors may offer the same product with different prices and higher minimum orders.	• Digikey • In stock (21/03/2024) • Min. order - 1134 uni • Price - 19642.20€ (1134 uni)
Development Kit	Yes	Yes	Yes	-
Suport	• High Support • Documentation and direct support from ST (including meetings and emails)	• Partial • Abundant documentation, however limited direct support	• Basic documentary support • An NDA is likely required	• Basic documentary support • An NDA is likely required

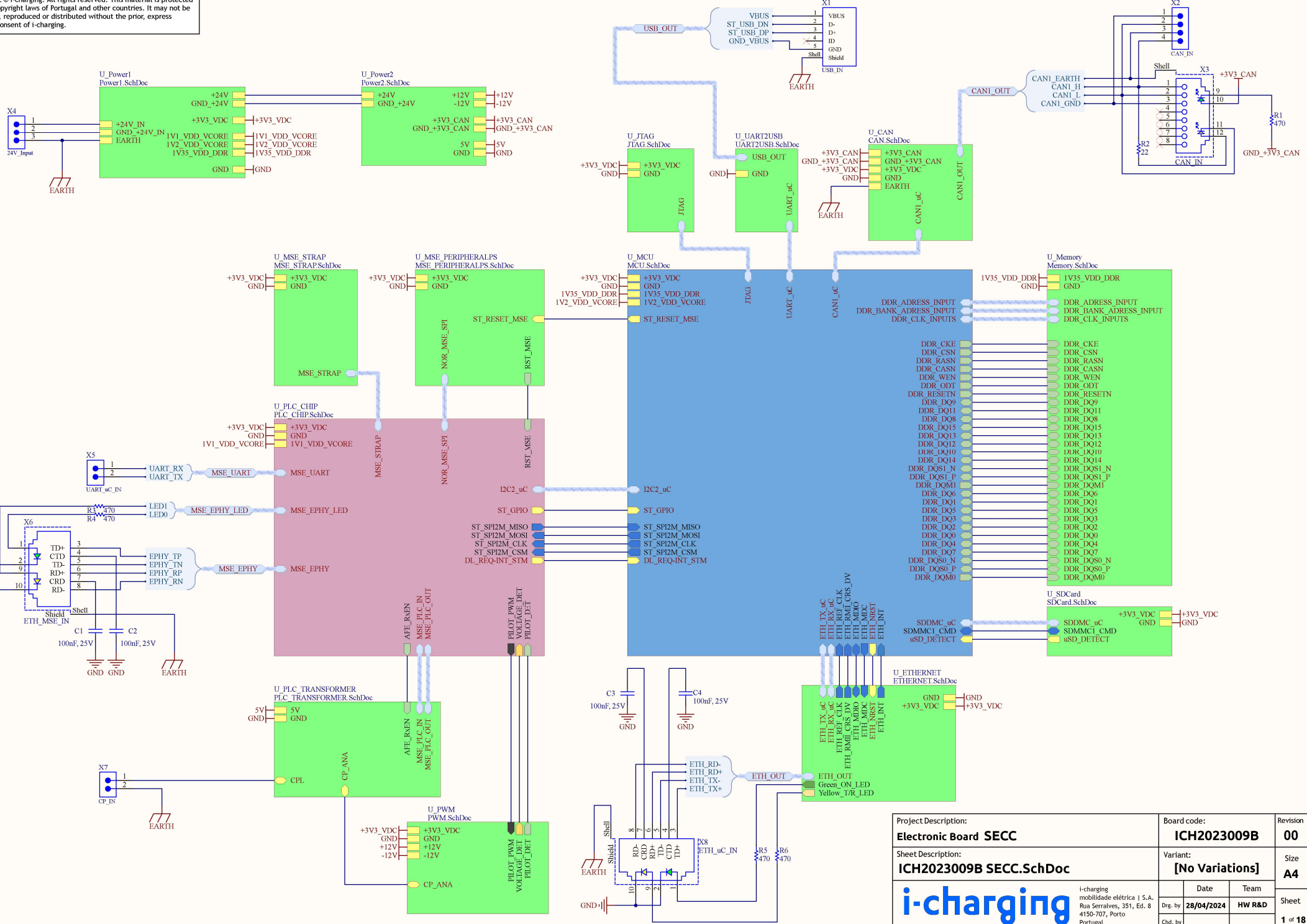
C.2 PLC Chip Comparison

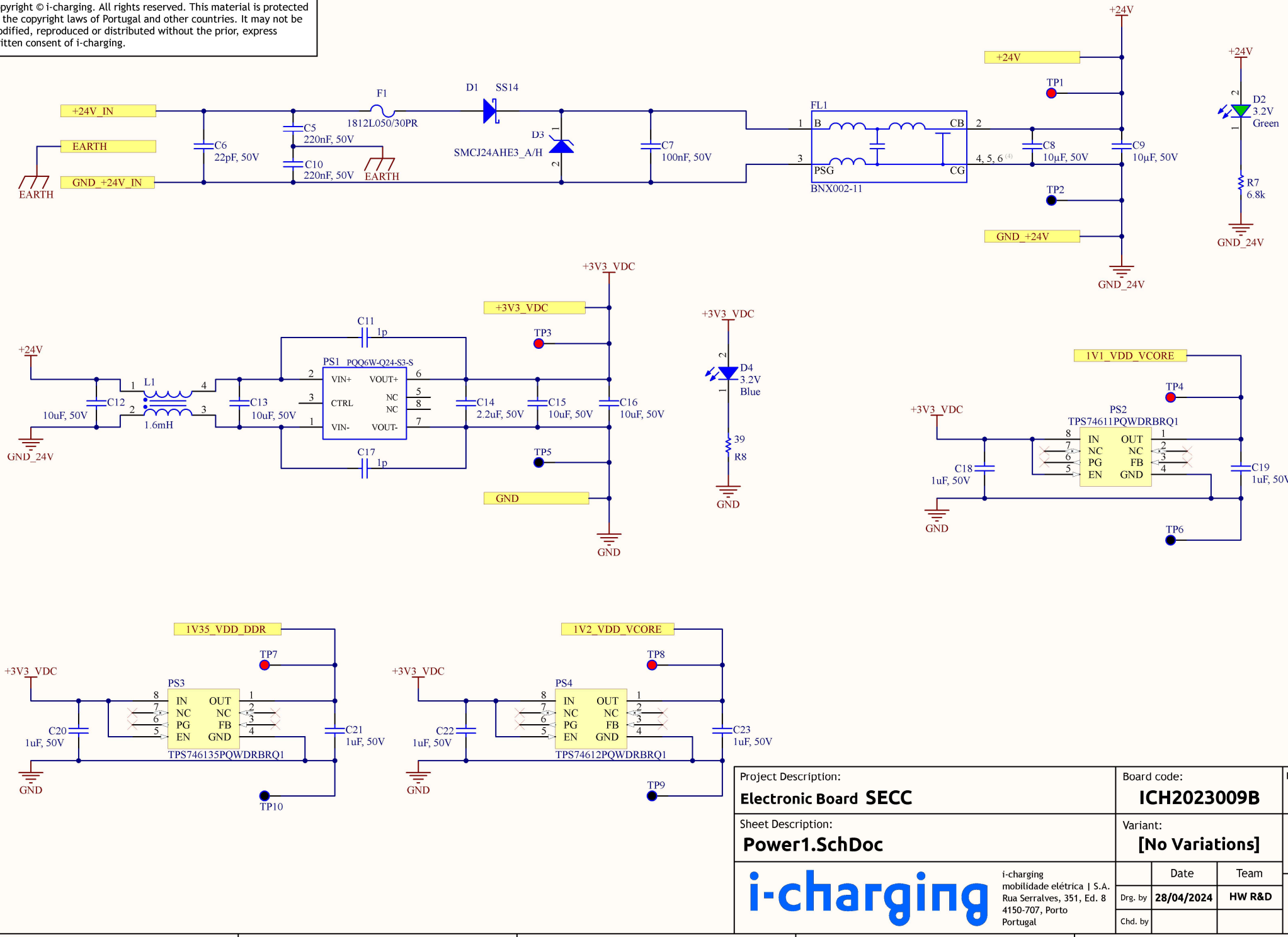
The following page present a comparison table of the three PLC chips initially considered for this project. The information pertaining to each cell was obtained from the official product briefs PDFs of the respective PLC chips, namely the QCA7000/7005 [28], IS32CG5317 [29] and MSE1021 [30].

Note: This comparison is based solely on documents available online. Information may be limited or unavailable for certain features.			
Part Number	**QCA7000/7005**	**IS32CG5317**	**MSE1021**
Manufacturer	Qualcomm	Lumissil	VertexCom
Compliant with ISO 15118	• HomePLug Green Phy • ISO 15118 / DIN 70121	• HomePLug Green Phy • ISO 15118 / DIN 70121	• HomePLug Green Phy • ISO 15118 / DIN 70121
Operating temperature	-40°C to 85°C	-40°C to 105°C	-40°C to 85°C
Conectivity	• Ethernet • UART • SPI • 4x General Purpose I/Os	• Ethernet • UART • SPI • JTAG • General Purpose I/Os	• Ethernet • 2x UART • SPI • 15x General Purpose I/Os
Package	QFN, 68 pins, 8×8 mm	EP-LQFP 80-pin package	EP-LQFP-80 10x10 mm
Oscillator	Single external 25 MHz crystal	Single external 25 MHz crystal	Single external 25 MHz crystal
Boot	Boot from host or external FLASH memory	Boot from host or external FLASH memory	Boot from host or external FLASH memory
Encryption	-	Yes	Yes
External line driver	-	Yes	Yes
PWM Generator	-	No	Yes
Availability, pricing, and suppliers	• VYRIAN Quotation: - In stock (09/05/2023); - 5 unities; - 70€ • 1 unity available, but way more expensive	• Mouser: - In stock (22/03/204); - 1 unity; - 12,32€. • Arrow: - Samples available (after meeting)	• Vertex Quotation: - In stock (03/08/2023); - 1 unity; • 54€ (Small quantity handling fee)
Support	• Only a flyer and a 54-page datasheet with some crucial information (QCA7000). • Software development support and application documentation are not provided unless large quantities are ordered.	• Datasheet, application notes, and access to development kit schematics provided. • Software and firmware development support is not provided if the development kit is not purchased.	• Datasheet, application notes, and access to development kit schematics • Software and firmware development support provided

Appendix D

SECC Prototype Circuit





Project Description: **Electronic Board SECC**	Board code: **ICH2023009B**	Revision **00**
Sheet Description: **Power1.SchDoc**	Variant: **[No Variations]**	Size **A4**

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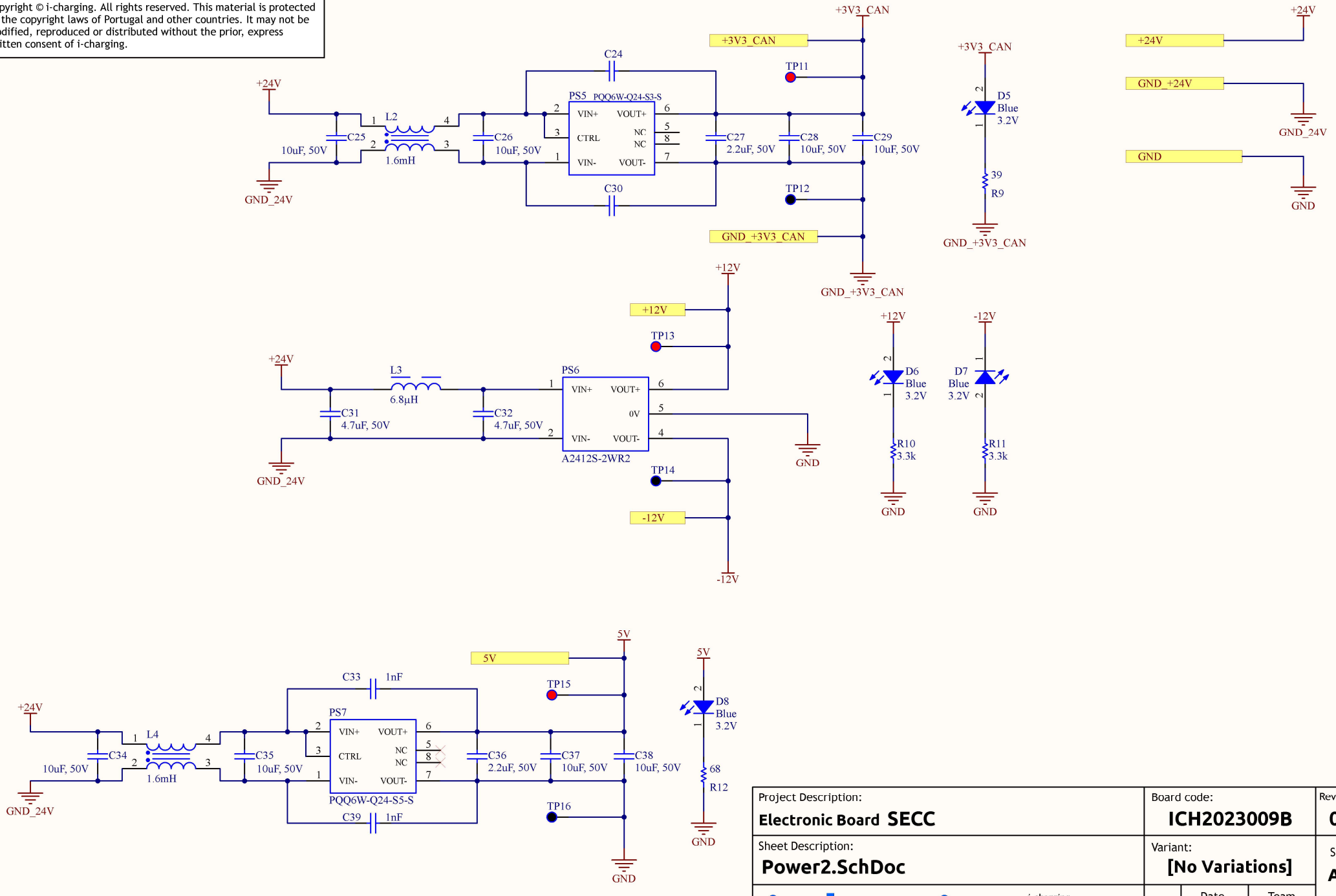
Portugal

	Date	Team
Drg. by	28/04/2024	HW R&D
Chd. by		

Sheet **2** of **18**



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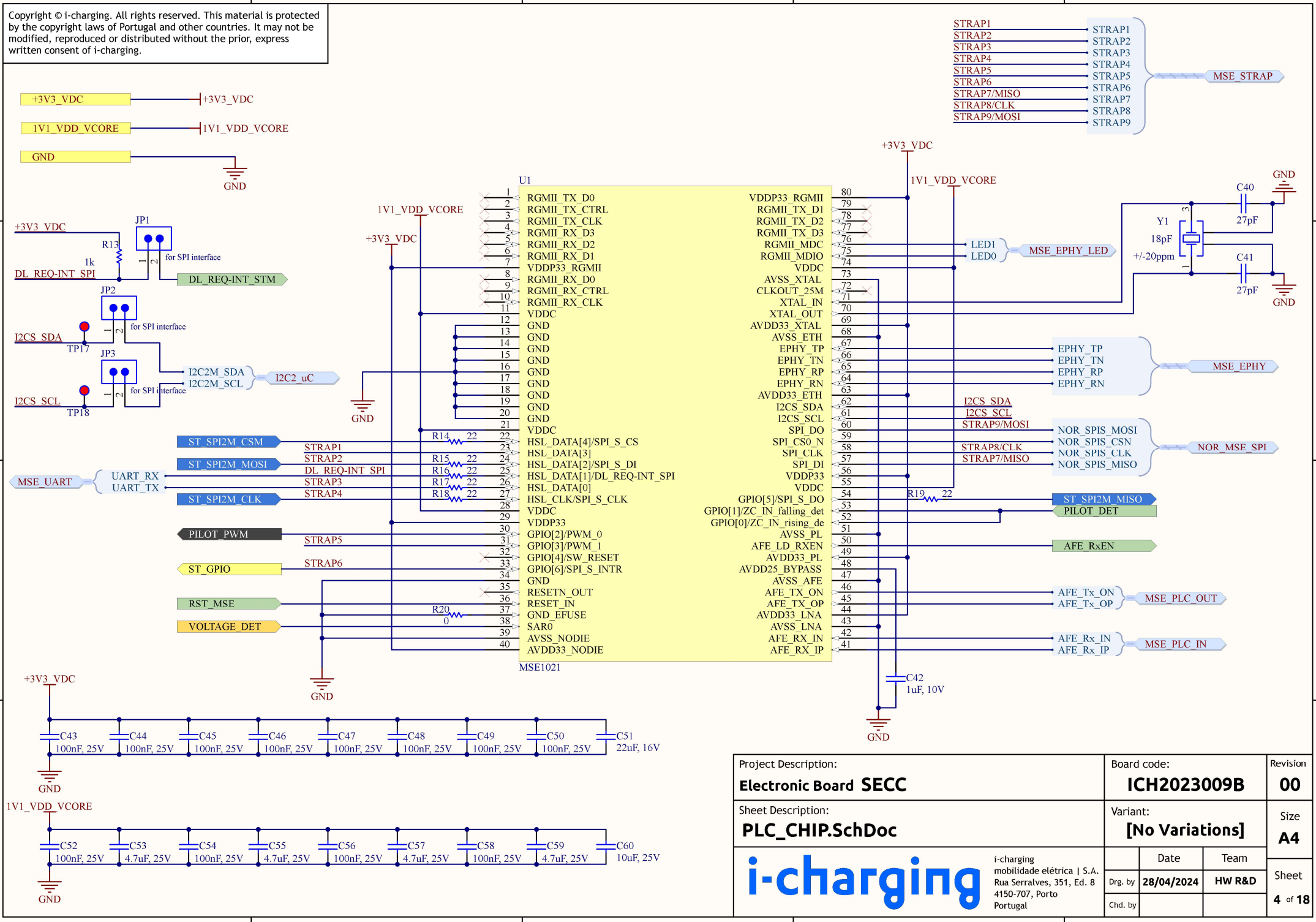
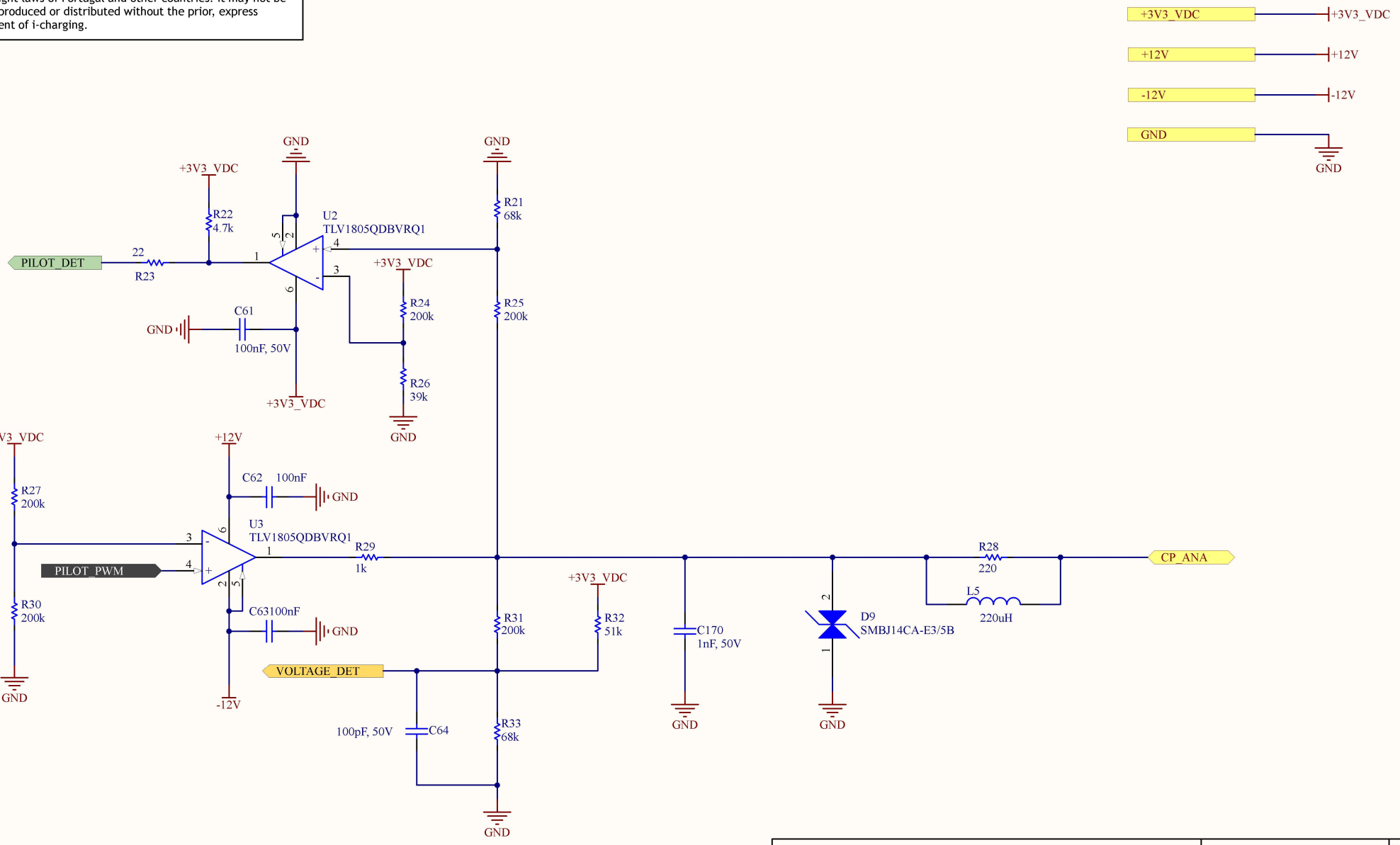
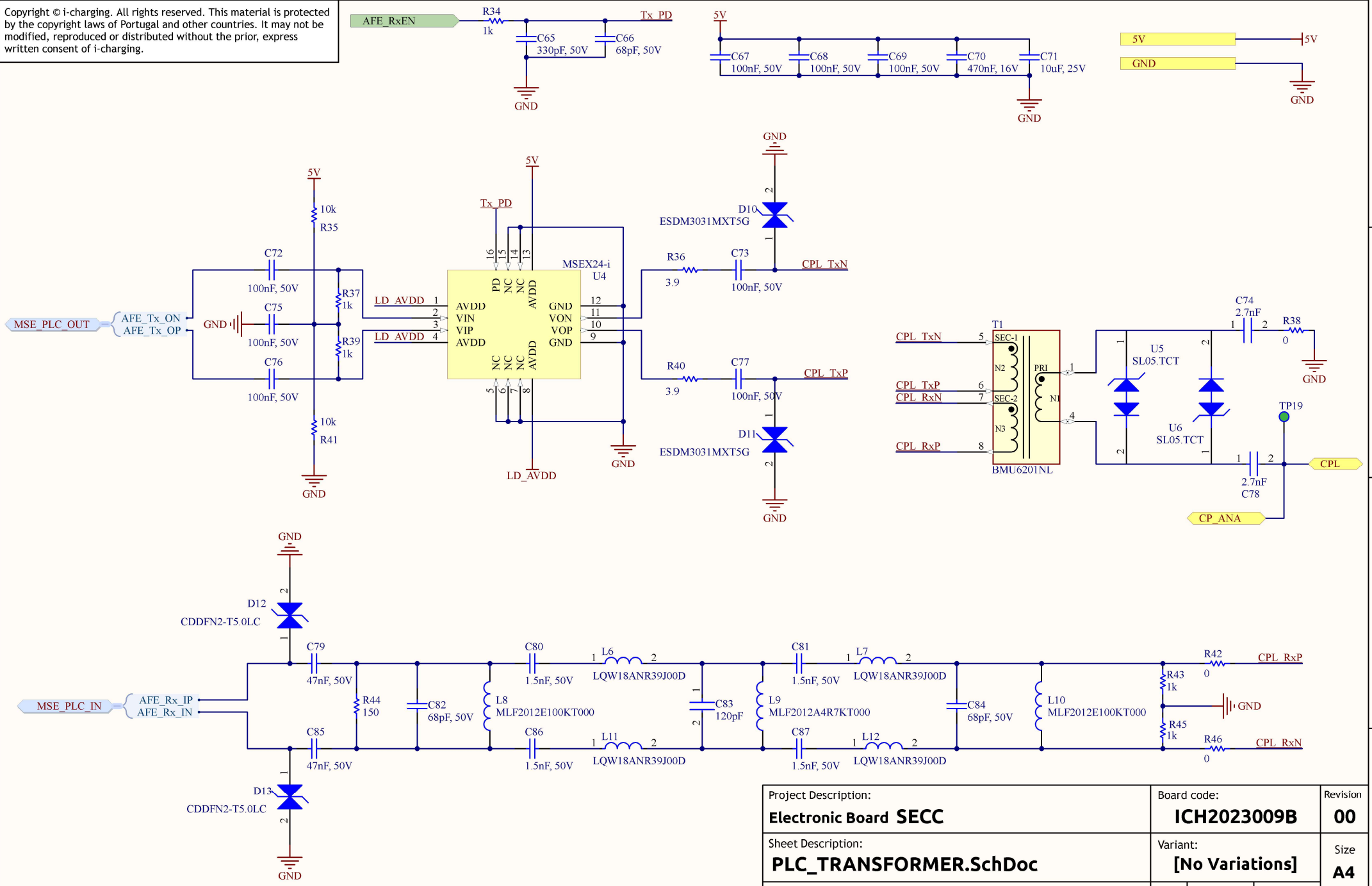
i-charging i-charging mobilidade elétrica | S.A. Rua Serralves, 351, Ed. 8 4150-707, Porto Portugal	Drg. by: Date **28/04/2024** Team **HW R&D** Chd. by:	Sheet **3** of **18**



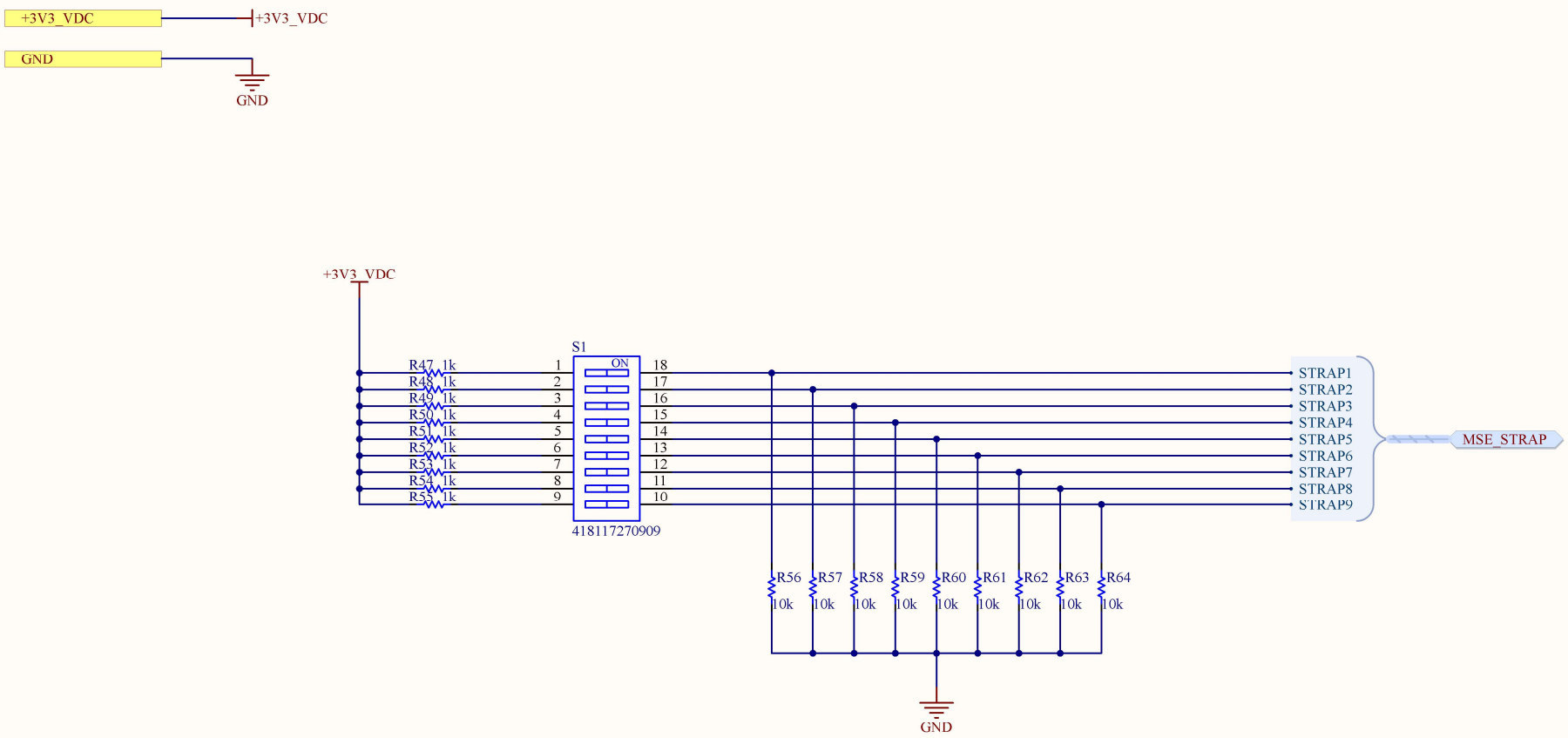
Project Description: **Electronic Board SECC**	Board code: **ICH2023009B**	Revision **00**
Sheet Description: **PLC_CHIP.SchDoc**	Variant: **[No Variations]**	Size **A4**
i-charging mobilidade elétrica | S.A. Rua Serralves, 351, Ed. 8 4150-707, Porto Portugal	Drg. by 28/04/2024 HW R&D; Chd. by	Sheet **4** of **18**



Project Description: **Electronic Board SECC**		Board code: **ICH2023009B**	Revision **00**
Sheet Description: **PWM.SchDoc**		Variant: **[No Variations]**	Size **A4**
i-charging	i-charging mobilidade elétrica | S.A. Rua Serralves, 351, Ed. 8 4150-707, Porto Portugal	Date / Team	Sheet **5** of **18**
		Drg. by **28/04/2024** **HW R&D**	
		Chd. by	



Project Description: **Electronic Board SECC**	Board code: **ICH2023009B**	Revision **00**
Sheet Description: **PLC_TRANSFORMER.SchDoc**	Variant: **[No Variations]**	Size **A4**
i-charging mobilidade elétrica | S.A.	Date / Drg. by **28/04/2024** / Team **HW R&D** / Chd. by	Sheet **6** of **18**



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Sheet Description: **MSE_STRAP.SchDoc**		Variant: **[No Variations]**	Size **A4**
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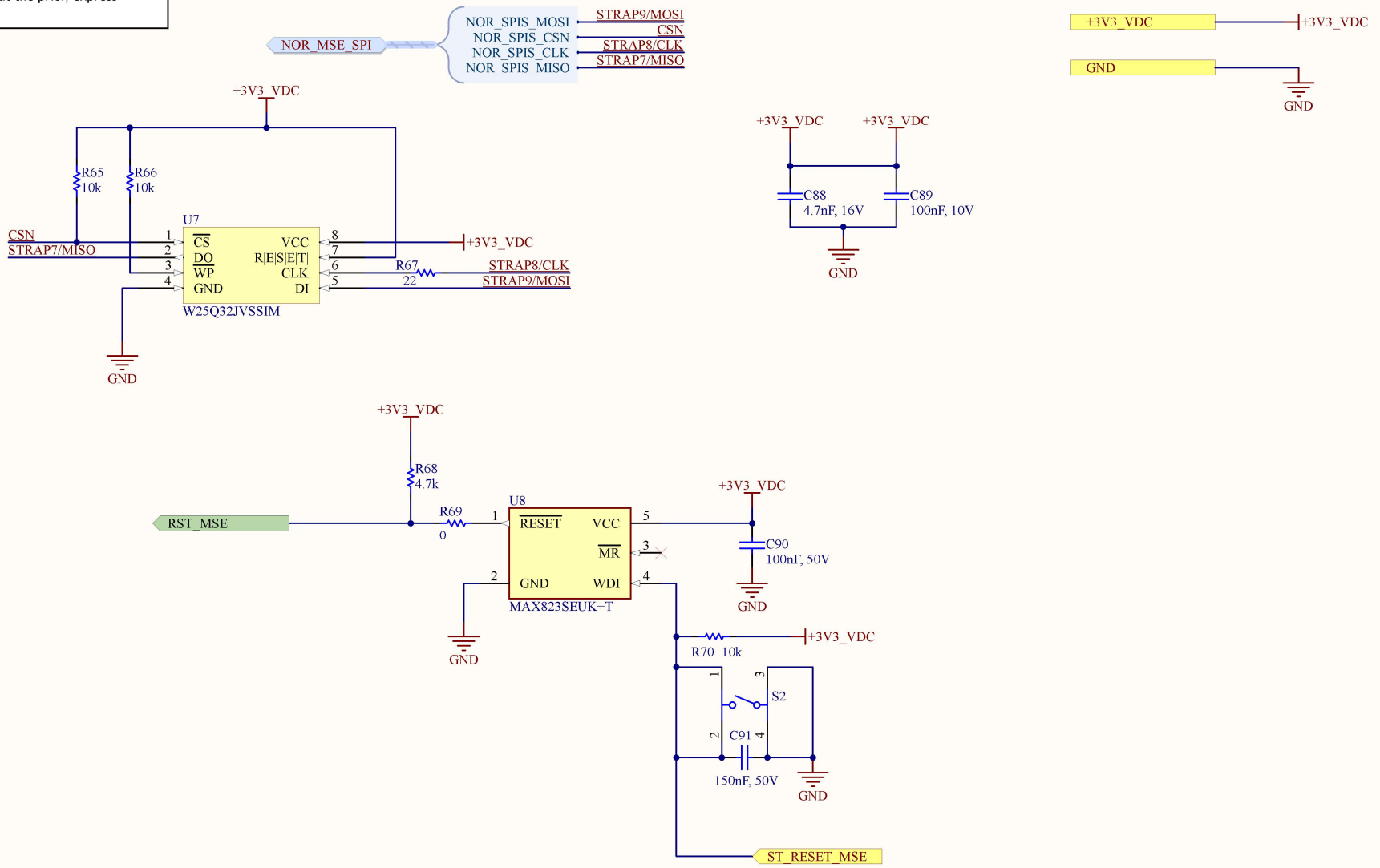
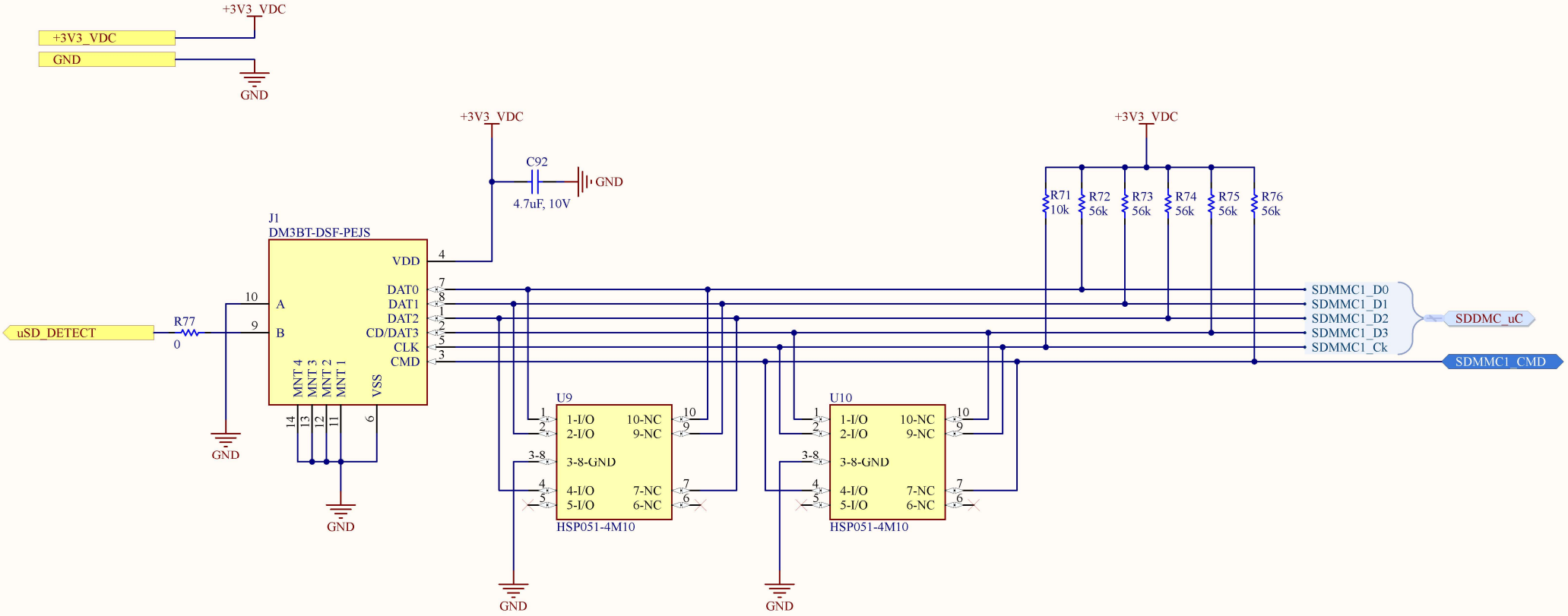
		Chd. by:	



Project Description: **Electronic Board SECC**		Board code: **ICH2023009B**	Revision **00**
Sheet Description: **MSE_PERIPHERALPS.SchDoc**		Variant: **[No Variations]**	Size **A4**
i-charging — i-charging mobilidade elétrica | S.A.		Date / Team	Sheet **8** of **18**
	Drg. by	**28/04/2024** / **HW R&D**	
	Chd. by		



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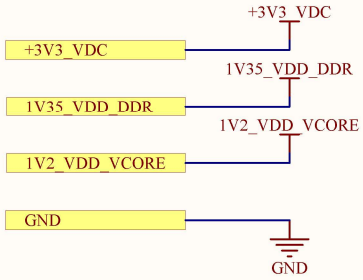
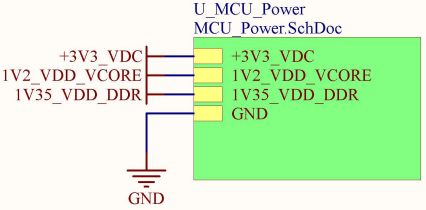
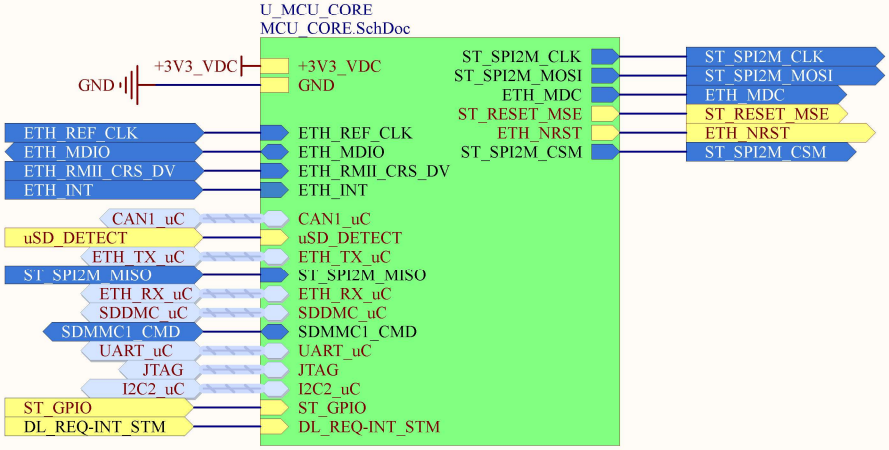
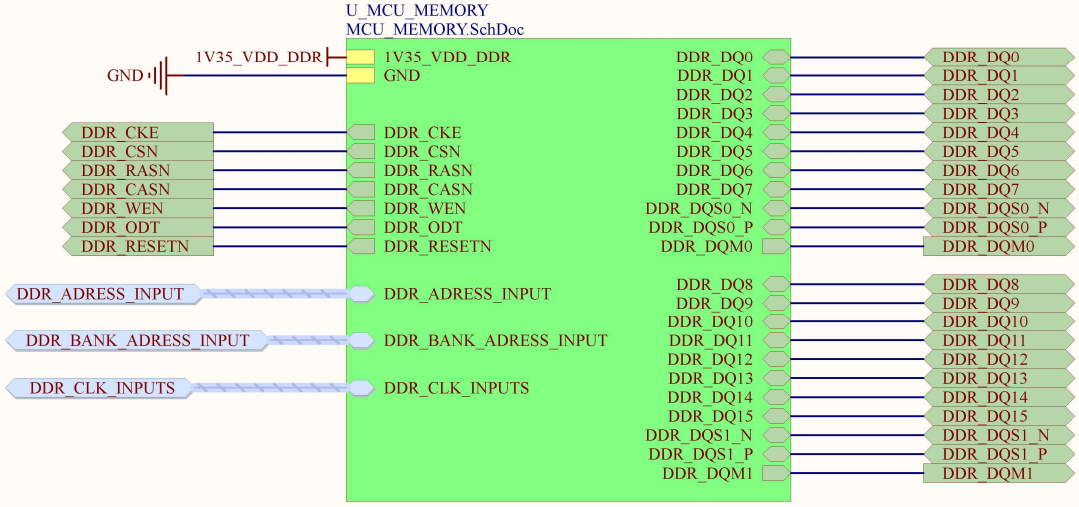
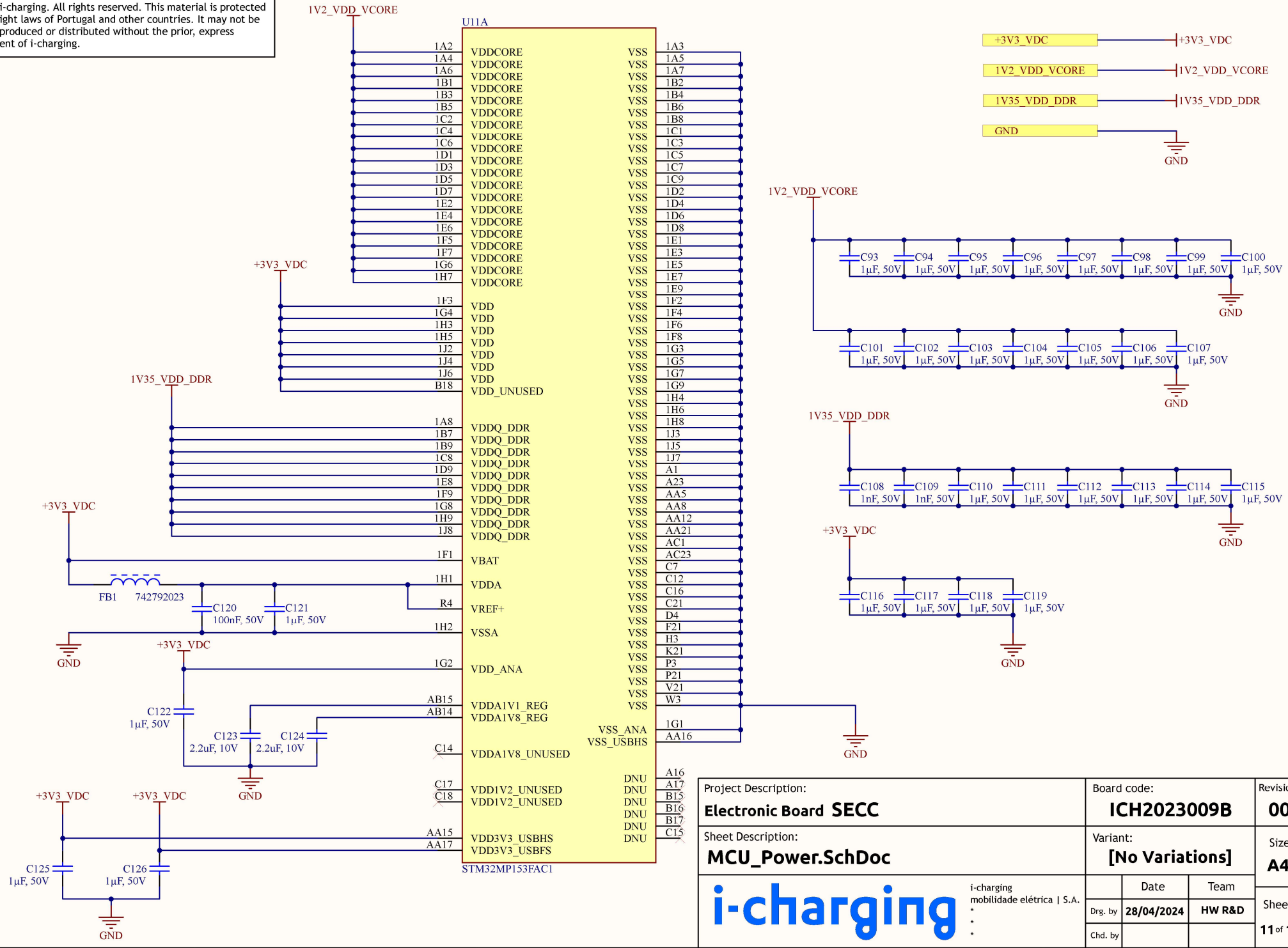








Project Description: **Electronic Board SECC**	Board code: **ICH2023009B**	Revision **00**
Sheet Description: **MCU.SchDoc**	Variant: **[No Variations]**	Size **A4**
i-charging mobilidade elétrica | S.A.	Date / Team	Sheet **10 of 18**
	Drg. by **28/04/2024** **HW R&D**	
	Chd. by	



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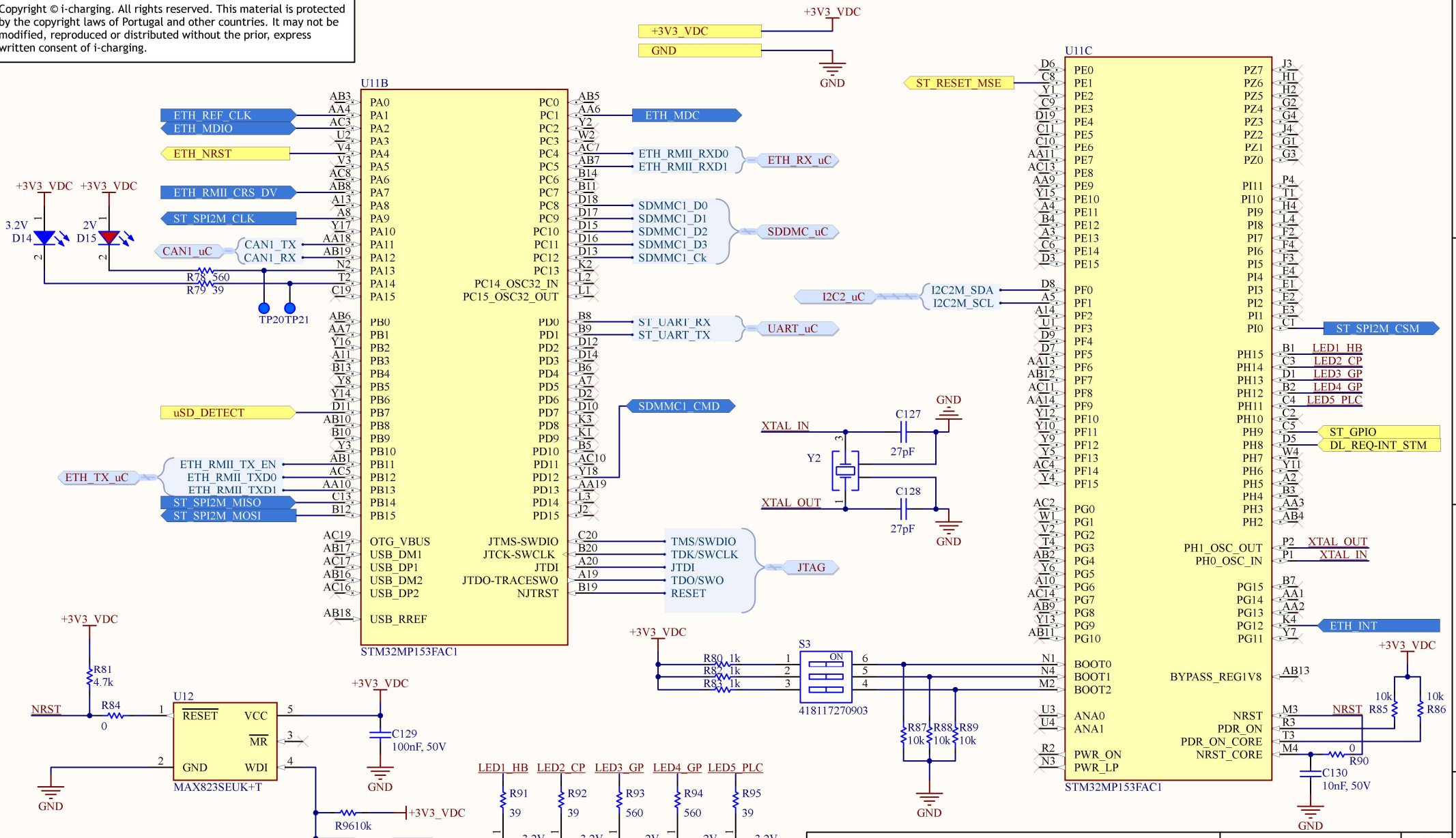
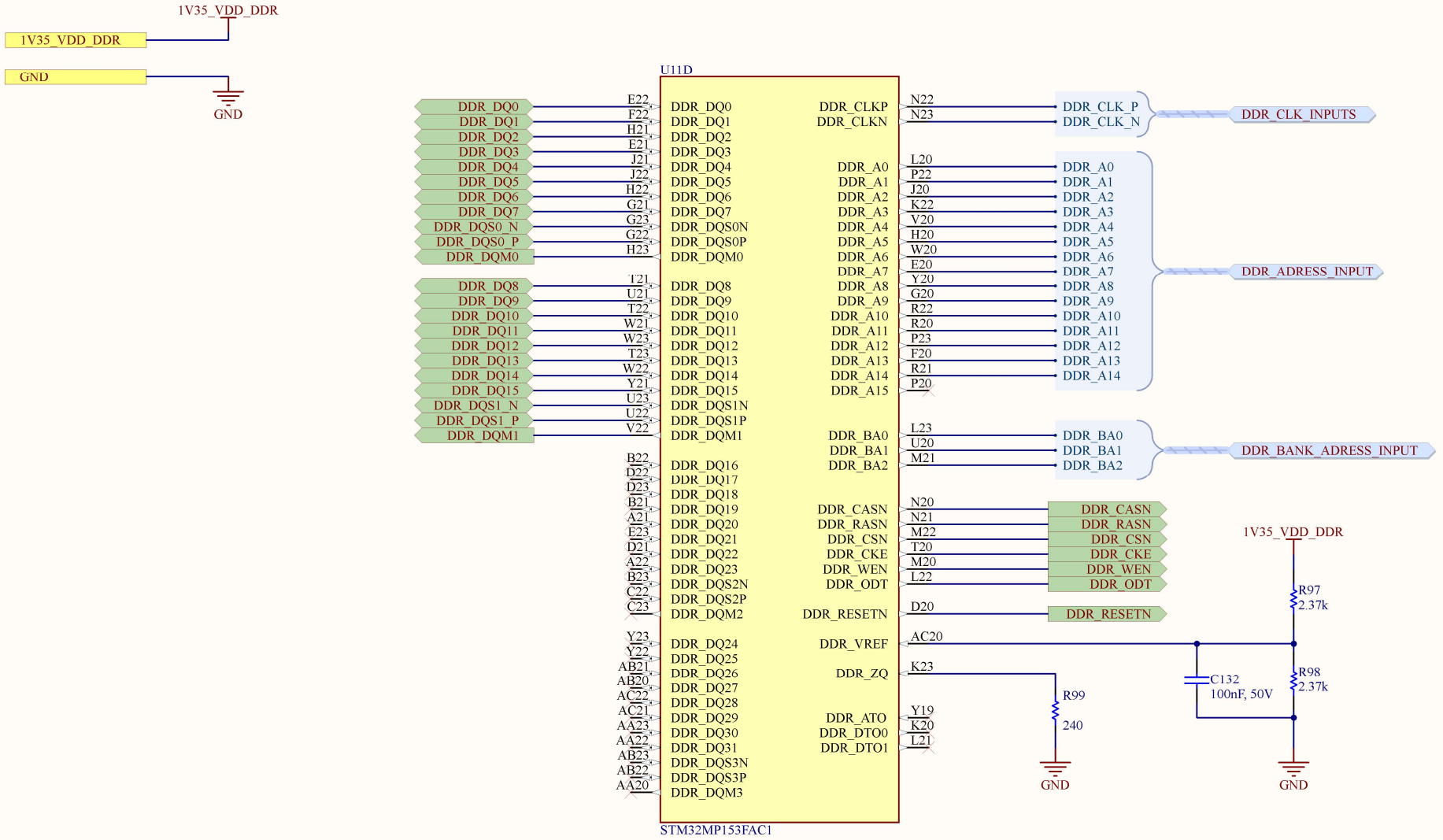
Sheet Description: **MCU_Power.SchDoc**		Variant: **[No Variations]**	Size **A4**
i-charging mobilidade elétrica | S.A.			Sheet **11** of **18**
	Date	Team	
Drg. by	28/04/2024	HW R&D	
Chd. by			



Project Description: **Electronic Board SECC**	Board code: **ICH2023009B**	Revision **00**	
Sheet Description: **MCU_CORE.SchDoc**	Variant: **[No Variations]**	Size **A4**	
i-charging mobilidade elétrica | S.A.	Date / Team	Sheet **12 of 18**	
	Drg. by **28/04/2024** **HW R&D**		
	Chd. by		



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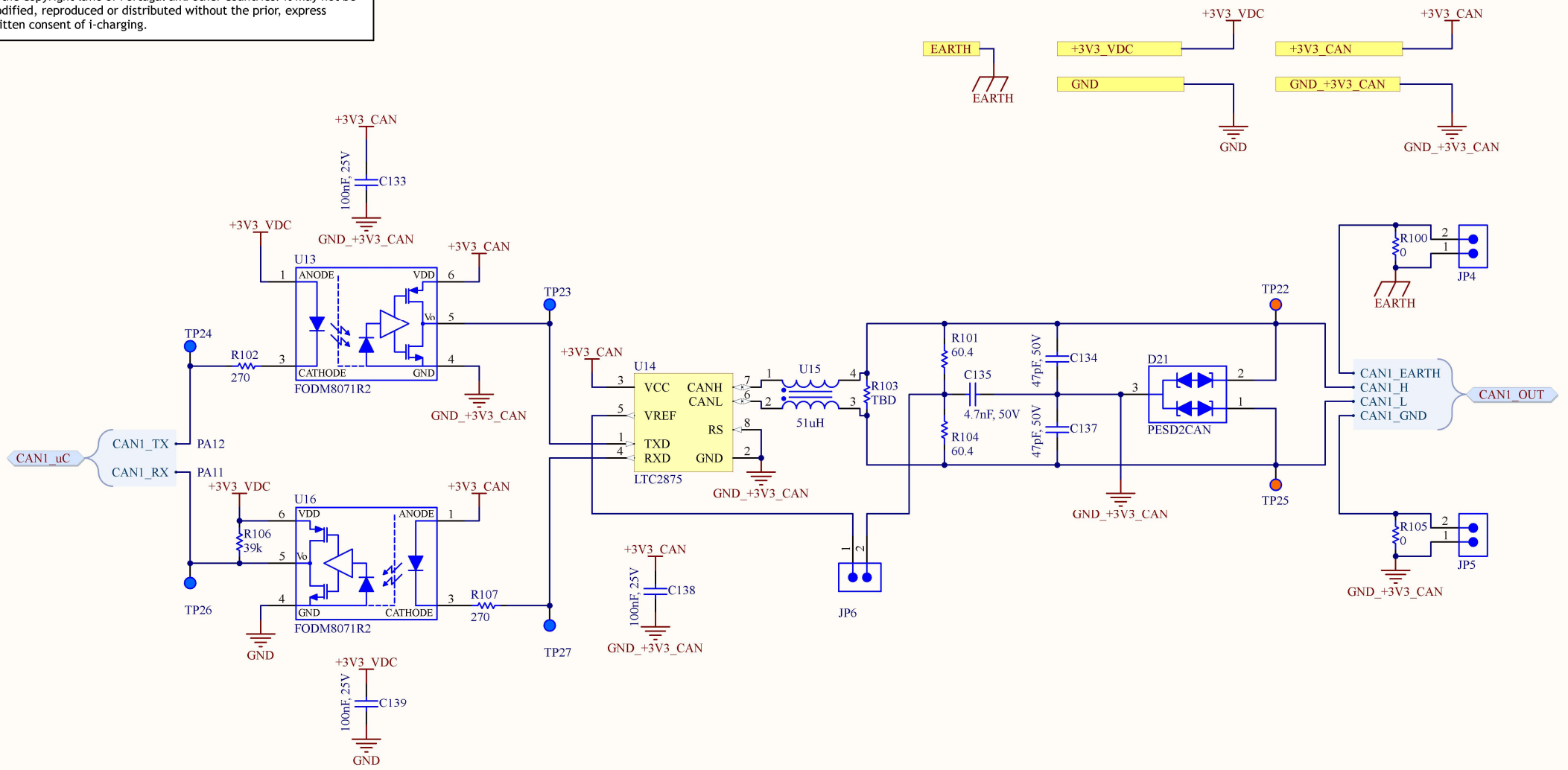
Sheet Description: **MCU_MEMORY.SchDoc**		Variant: **[No Variations]**	Size **A4**
i-charging mobilidade elétrica | S.A.	Date	Team	Sheet **13** of **18**
	Drg. by **28/04/2024**	**HW R&D**	
	Chd. by		



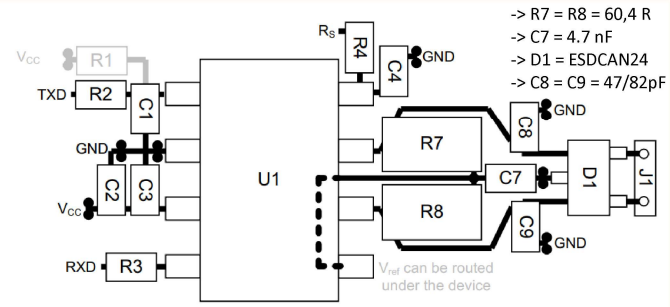
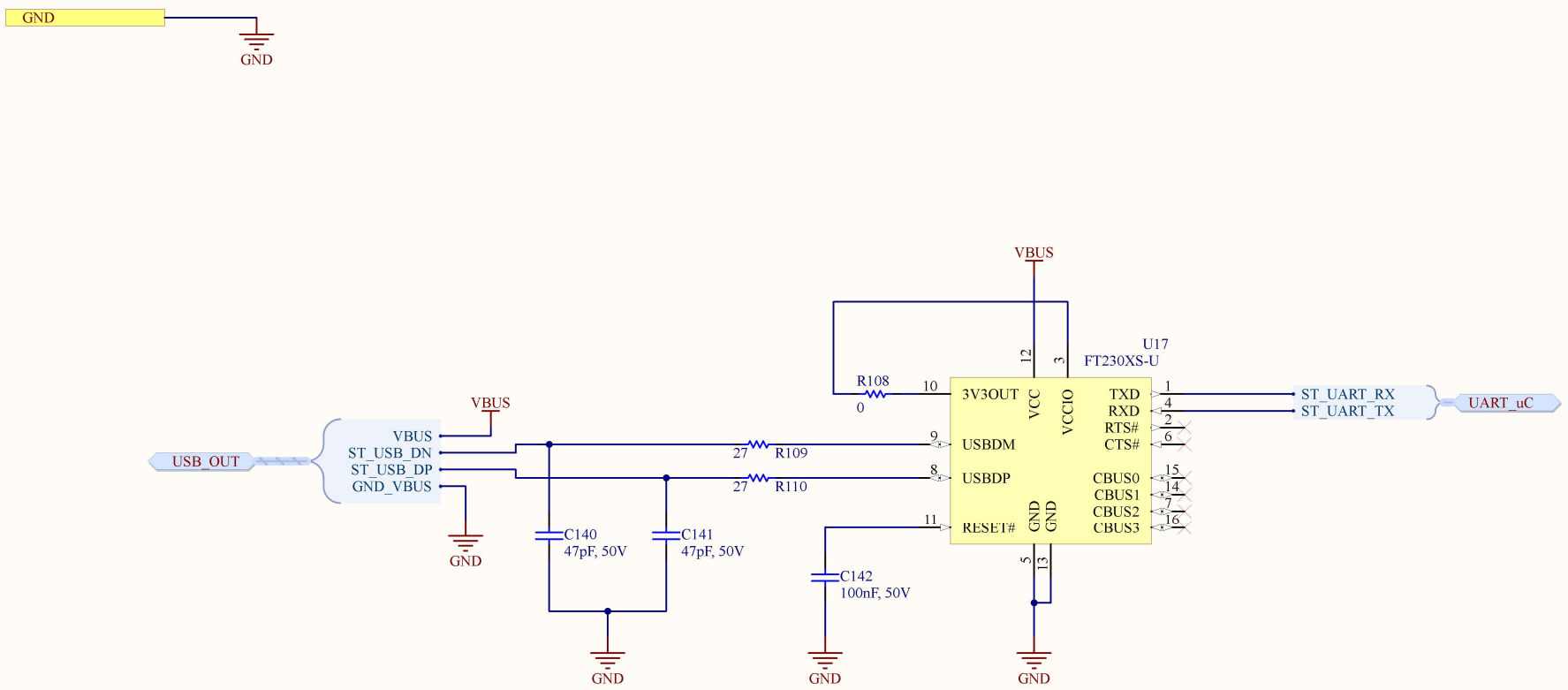
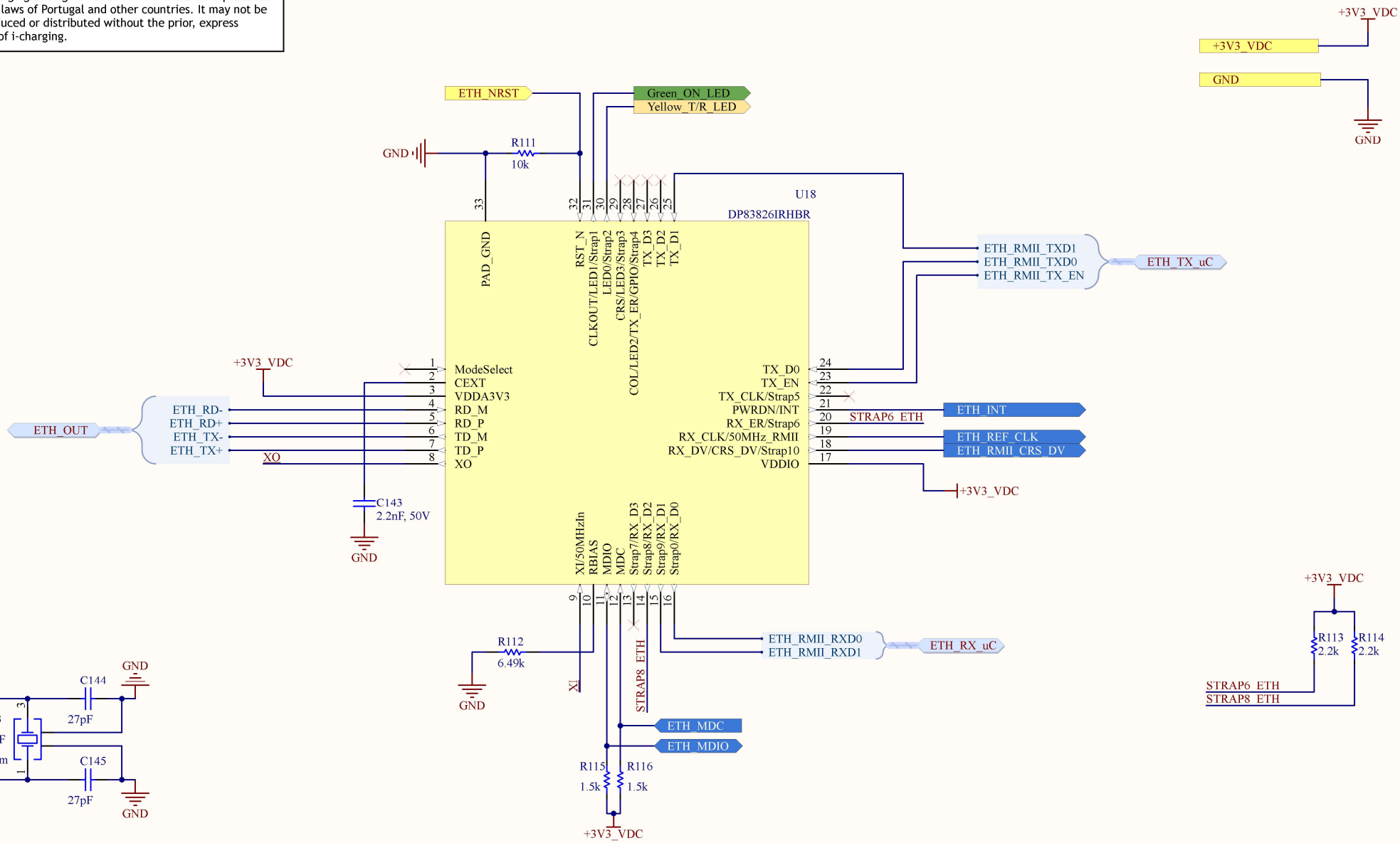


Figure 44. SN65HVD23x Board Layout

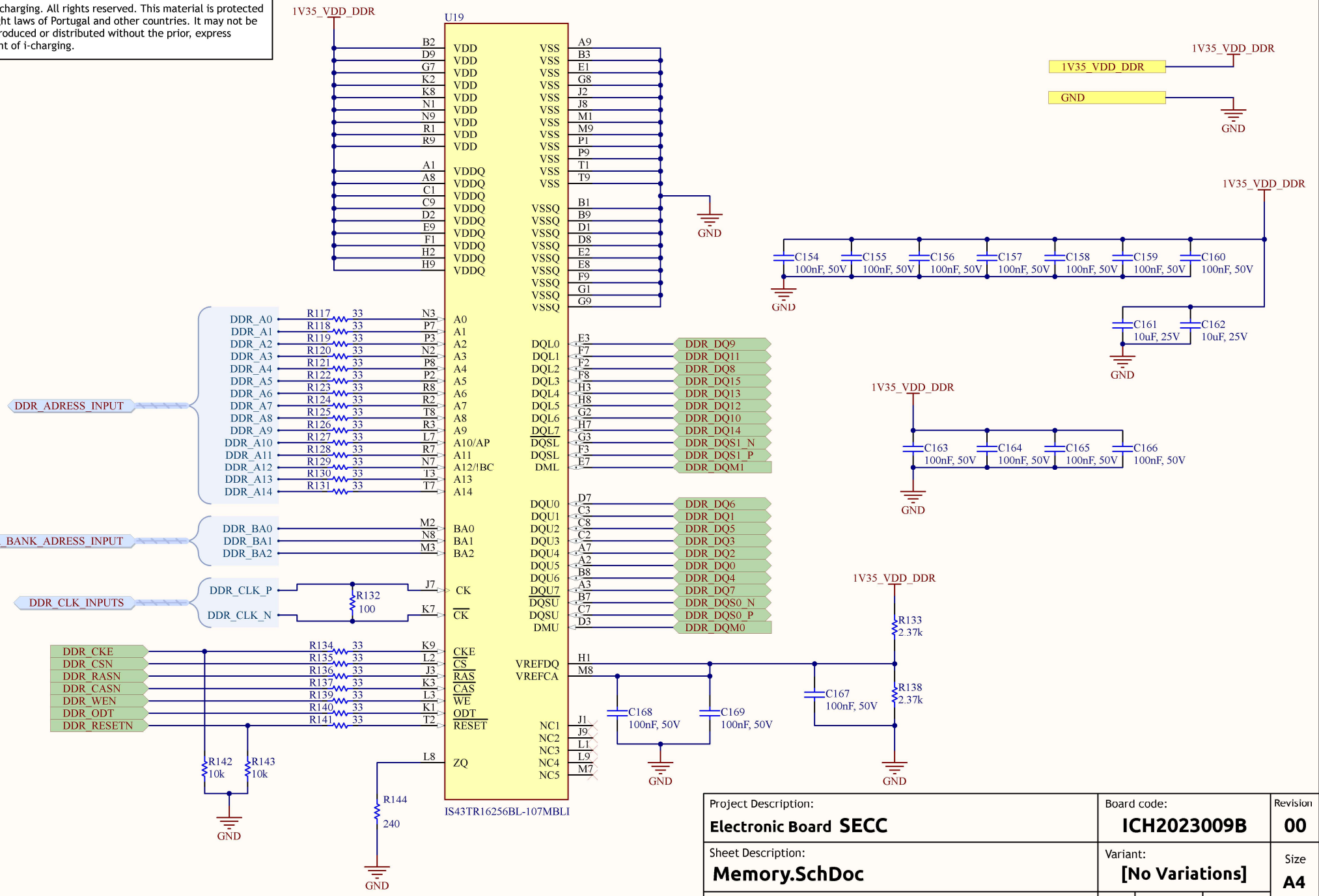
Project Description: **Electronic Board SECC**		Board code: **ICH2023009B**	Revision **00**
Sheet Description: **CAN.SchDoc**		Variant: **[No Variations]**	Size **A4**
i-charging	i-charging mobilidade elétrica | S.A.	Date / Team	Sheet **14** of **18**
		Drg. by **28/04/2024** **HW R&D**	
		Chd. by	



Project Description: **Electronic Board SECC**		Board code: **ICH2023009B**	Revision **00**
Sheet Description: **UART2USB.SchDoc**		Variant: **[No Variations]**	Size **A4**
i-charging mobilidade elétrica | S.A.	Date	Team	Sheet **15** of **18**
	Drg. by **28/04/2024**	**HW R&D**	
	Chd. by		



Project Description: **Electronic Board SECC**	Board code: **ICH2023009B**	Revision **00**	
Sheet Description: **ETHERNET.SchDoc**	Variant: **[No Variations]**	Size **A4**	
i-charging mobilidade elétrica | S.A.	Date / Team	Sheet **16 of 18**	
	Drg. by **28/04/2024** **HW R&D**		
	Chd. by		



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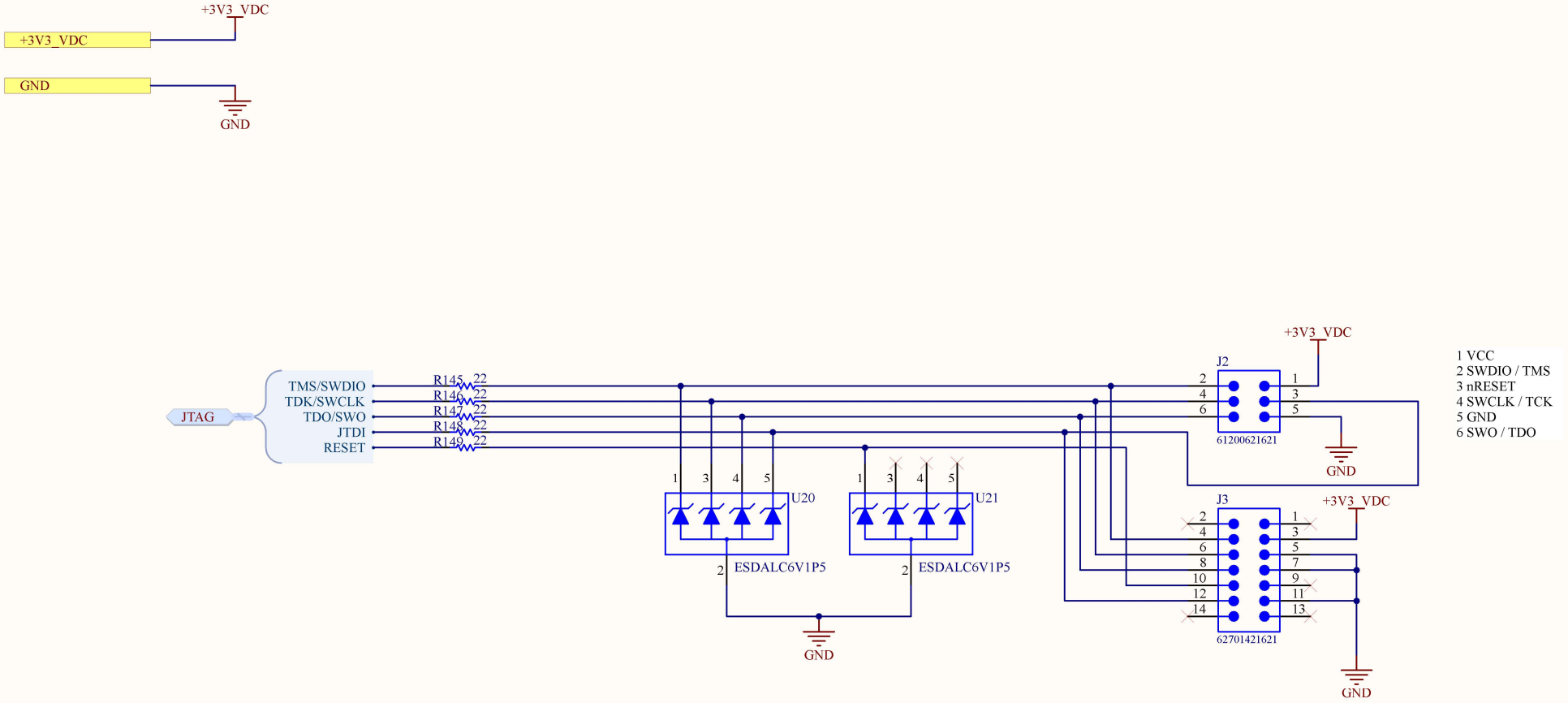
Sheet Description: **Memory.SchDoc**	Variant: **[No Variations]**	Size **A4**	
i-charging mobilidade elétrica | S.A.	Date / Team	Sheet **17 of 18**	
	Drg. by **28/04/2024** **HW R&D**		
	Chd. by		



Project Description: **Electronic Board SECC**	Board code: **ICH2023009B**	Revision **00**	
Sheet Description: **JTAG.SchDoc**	Variant: **[No Variations]**	Size **A4**	
i-charging i-charging mobilidade elétrica | S.A. Rua Serralves, 351, Ed. 8 4150-707, Porto Portugal	Drg. by: Date **28/04/2024** Team **HW R&D** Chd. by:	Sheet **18** of **18**	